Cisco Embedded Service 6300 Series Router Hardware Technical Guide

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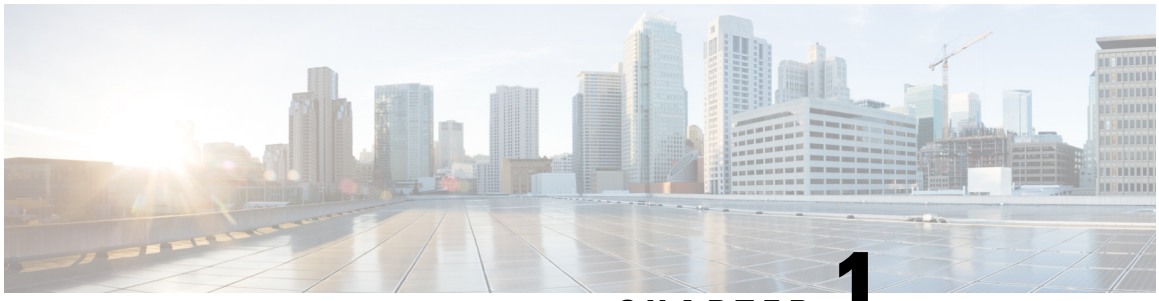
CONTENTS



CHAPTER 1

Product Overview

This chapter contains the following sections:

Overview

This hardware technical guide provides a product description, specifications, and compliance information for the Cisco Embedded Service 6300 Series Router.

The documentation set for this product strives to use bias-free language. For purposes of this documentation set, bias-free is defined as language that does not imply discrimination based on age, disability, gender, racial identity, ethnic identity, sexual orientation, socioeconomic status, and intersectionality. Exceptions may be present in the documentation due to language that is hardcoded in the user interfaces of the product software, language used based on RFP documentation, or language that is used by a referenced third-party product.

The ESR6300 is a compact form factor embedded router module with a board size of 3.0" x 3.775"(76.2mm x 95.885mm). This module *may* fit in an enclosure that was *originally designed* for PC/104 modules with some additional adaptation. The more compact design simplifies integration and offers system integrators the ability to use the Cisco ESR6300 in a wide variety of embedded applications. The ESR card is available with a Cisco-designed cooling plate customized to the ESR, as well as without the cooling plate for system integrators who want to design their own custom thermal solution.

Note More on the PC/104 standard can be found on the PC/104 Consortium website at https://pc104.org/

Note IOx development is not supported on the ESR6300. While this is platform independent code, it is unsupported and untested on this device.

The following table provides the hardware product IDs and brief descriptions for the boards.

SKU	Description	Ports/Module Interfaces
ESR-6300-NCP-K9	Embedded Router Board without a cooling plate. (NCP = No Cooling Plate)	4 GE LAN ports 2 combo GE WAN ports 1 USB 3.0 port 1 async UART port 1 alarm input 1 Pluggable module interface
ESR-6300-CON-K9	Embedded Router Board with cooling plate. (CON = Conduction cooled).	4 GE LAN ports 2 combo GE WAN ports 1 USB 3.0 port 1 async UART port 1 alarm input 1 Pluggable module interface

Audience

This guide is for system integrators who are integrating the Cisco ESR6300 into a custom end product.

General Description

The ESR6300 is a ruggedized GigE Embedded Router platform for tactical, outdoor and mobile installations. Some of the key features are:

- Daughter board compact form factor 3.0" x 3.775"(76.2mm x 95.885mm)
- Class A EMC
- Industrial Temperature: -40C to +85C conduction plate temperature range
- 3.3V and 5V power inputs
- ARM Quad-Core A72 CPU, 1200MHz
- 4GB DDR4 memory capacity (32-bit + 4-bit ECC)
- 4GB usable (pSLC mode) eMMC flash
- Anti-counterfeit chip and Secure Boot
- Temperature Sensor
- Power consumption and voltage monitoring
- Gigabit Ethernet LAN Switch for 4 external LAN ports
- Gigabit Ethernet WAN PHY for 2 external WAN combo ports
- Interface to external features (requires additional circuitry):
    - Four GE 10/100/1000 LAN Ports (with PoE support)
    - Two GE combo (10/100/1000 and SFP) WAN Ports
    - One UART interface (for RS232 async serial port with flow control)

- One UART Console interface (for CPU console access)
- RTC (Real Time Clock) with customer-provided battery backup
- Push Button that supports the Zeroize feature
- One dry contact alarm input
- One USB 3.0 Host interface (for USB Flash Memory Device)
- One Cisco supported Pluggable Module Interface (for 4G/LTE module support)

Note In order to recover the device from a complete zeroization, it must be configured with a Cisco supported USB3.0 device. Before triggering the zeroization process, make sure you are familiar with the topics in Device Zeroization, on page 51 and Configuration Reset Overview, on page 49!

Note The ESR6300 hardware uses GE as the name for the Gigabit Ethernet ports. However, Cisco IOS commands use Gi as the naming convention.

- Software: Cisco IOS-XE
- IPSec

ESR Board Layout and Dimensions

The following picture shows the ESR Board (left) with the cooling plate (right). The board dimensions are 3.0" x 3.775" (76.2mm x 95.885mm).

Board Without Cooling Plate

The following figures show the layout and dimensions of the ESR Board that is not equipped with the Cisco-designed cooling plate (ESR-6300-NCP-K9).

Note Dimensions in inches. Tolerances (unless otherwise stated): .XX +/- 0.010, .XXX +/- 0.005

Figure 1: ESR-6300-NCP-K9

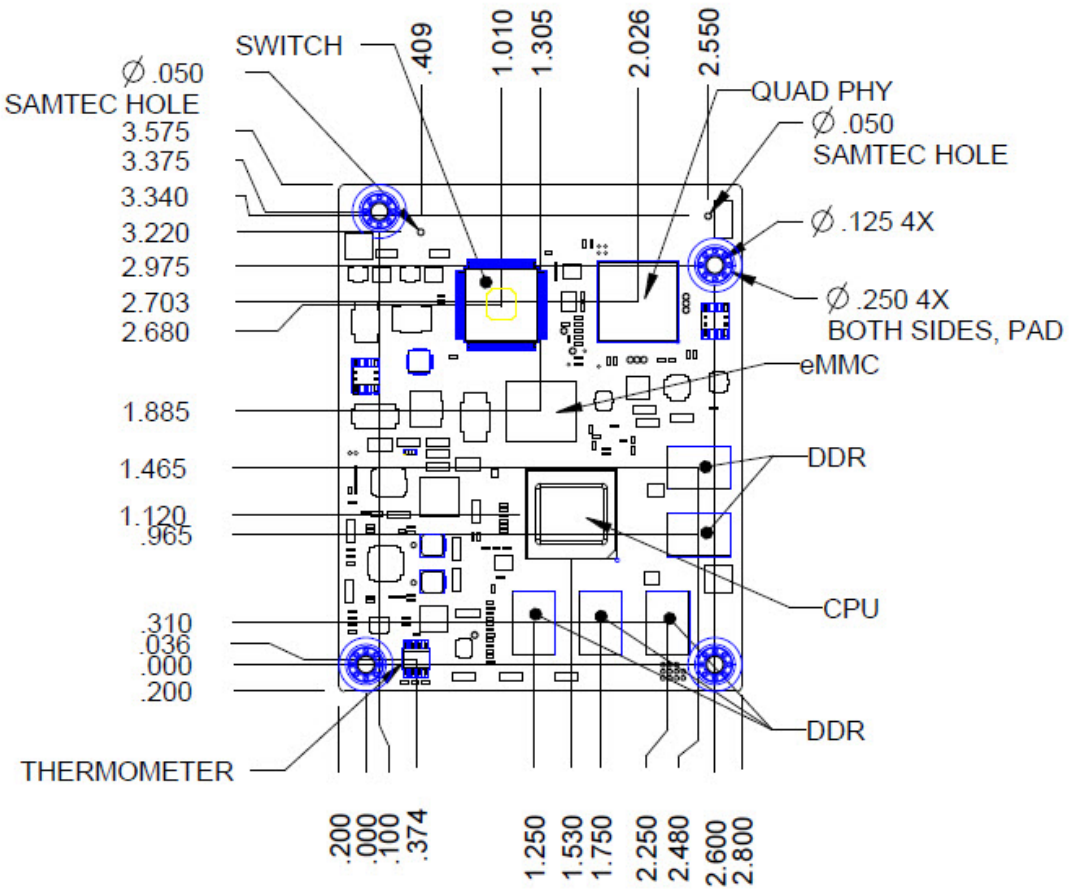


Figure 2: ESR-6300-NCP-K9

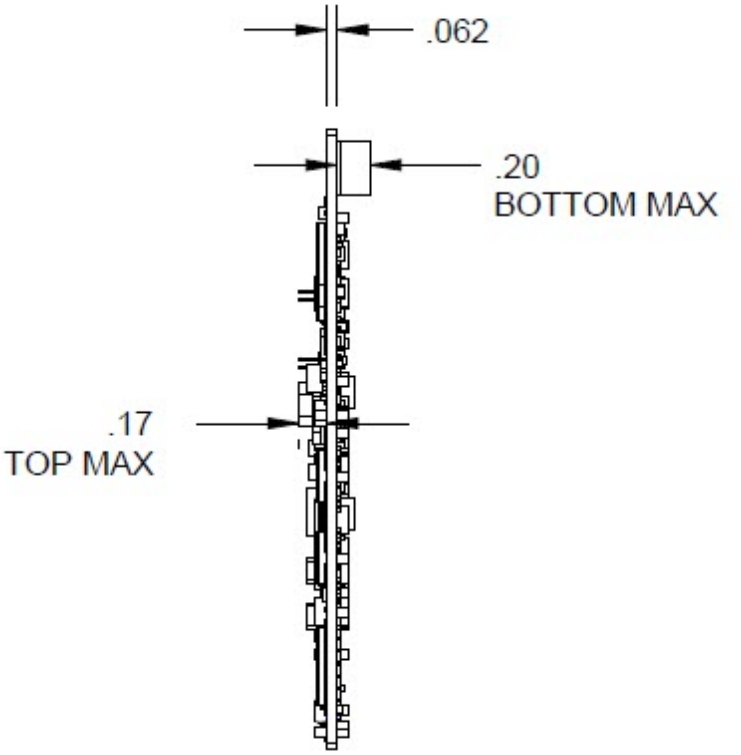
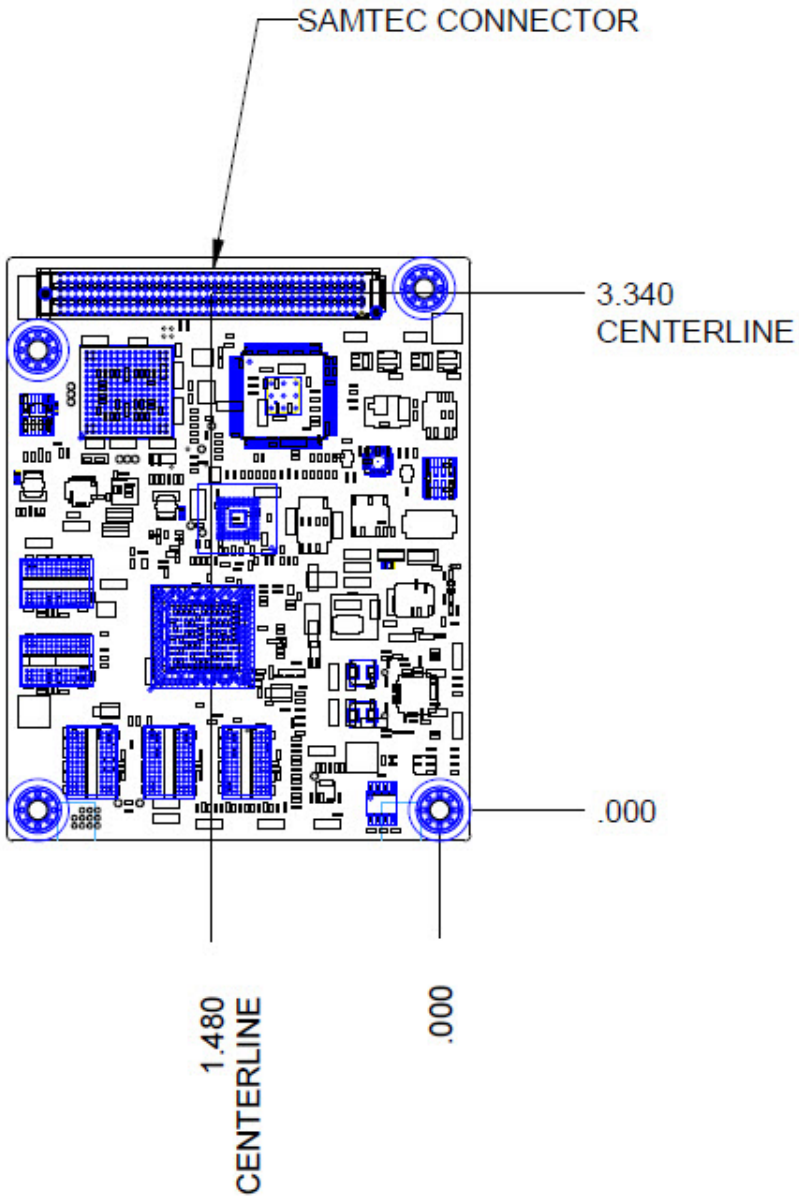


Figure 3: ESR-6300-NCP-K9



Board With Cooling Plate

The following figures show the layout and dimensions of the ESR Board that is equipped with the Cisco-designed cooling plate (ESR-6300-CON-K9).

Note Dimensions in inches. Tolerances (unless otherwise stated): .XX +/- 0.010, .XXX +/- 0.005

Figure 4: ESR-6300-CON-K9

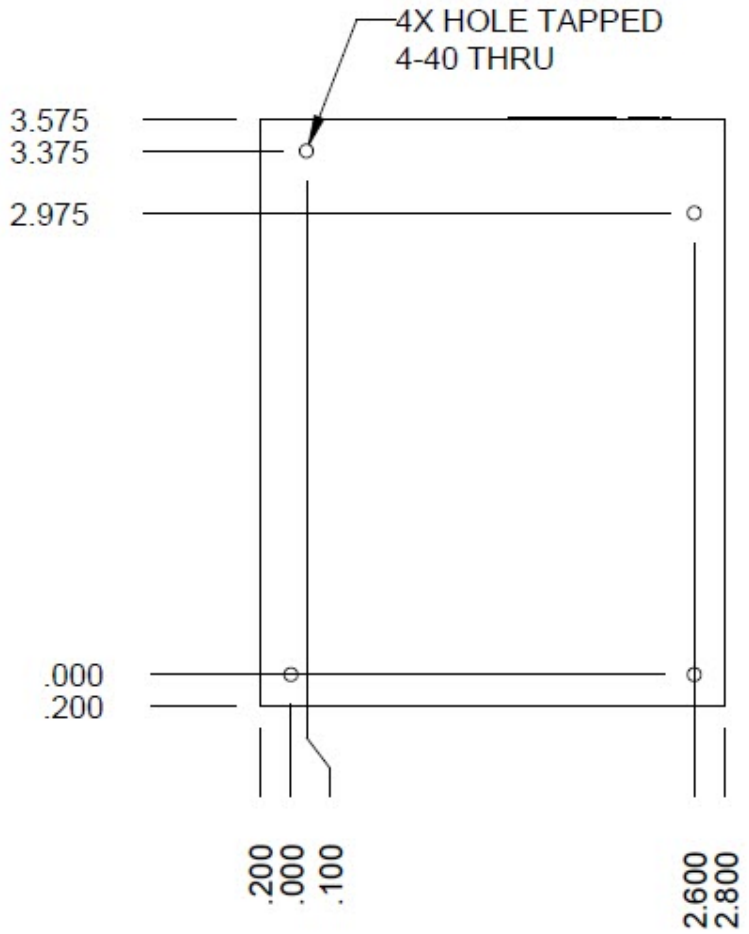


Figure 5: ESR-6300-CON-K9

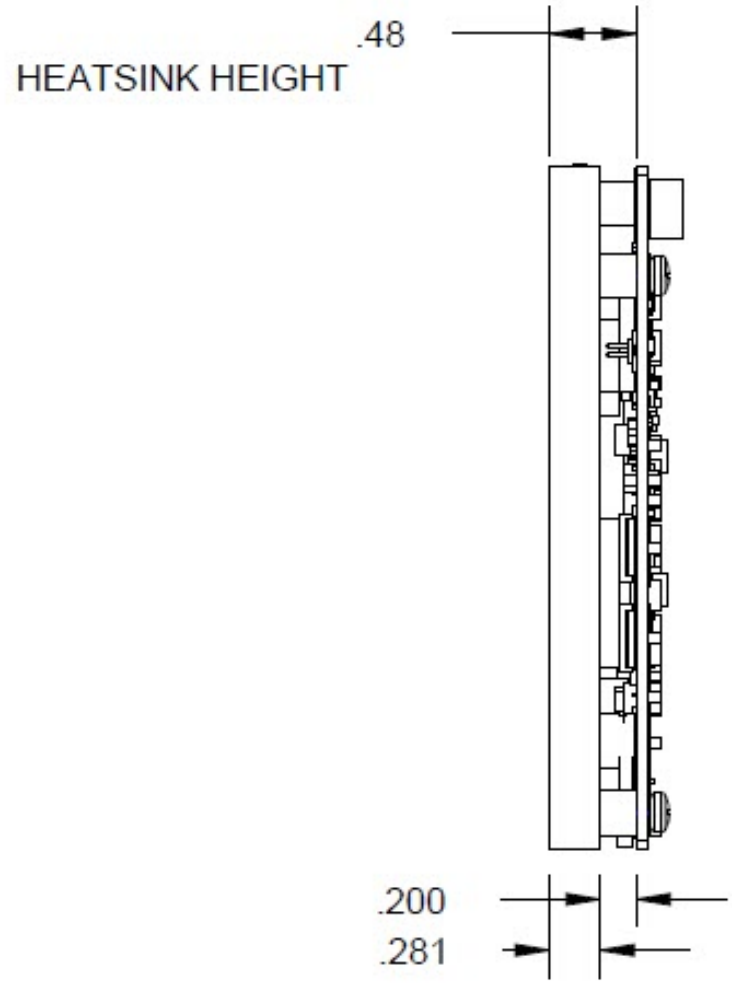
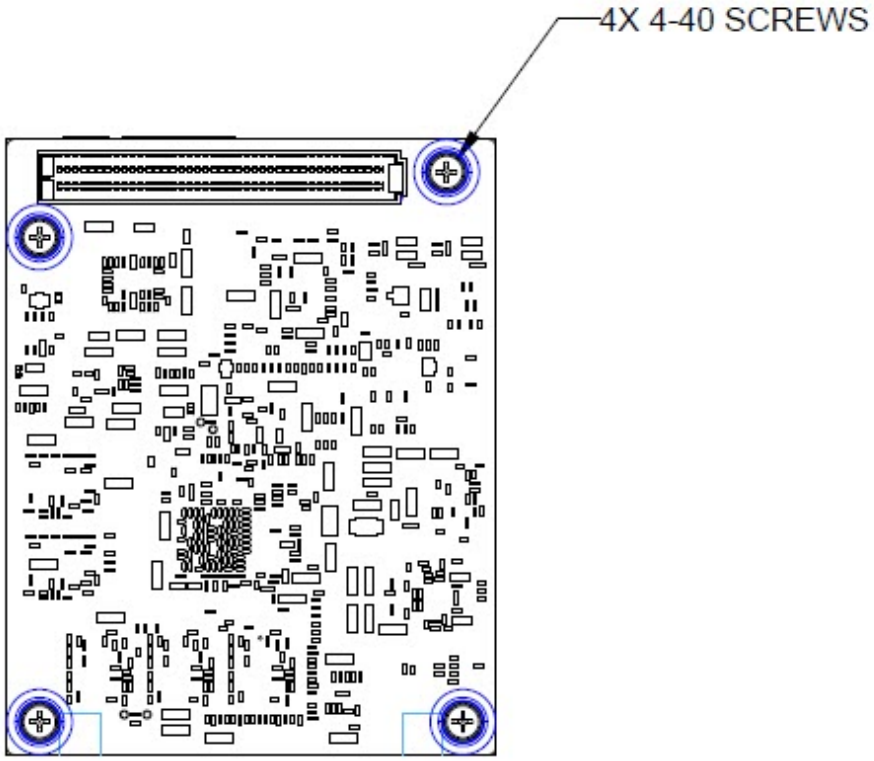


Figure 6: ESR-6300-CON-K9



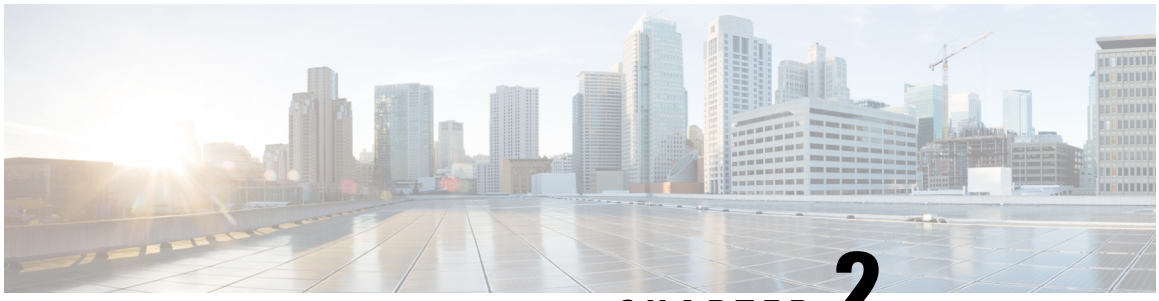
External USB 3.0

There is support for an external USB3.0 type A device built into the USB controller.

Important In order to recover the device from a complete zeroization, it must be configured with a Cisco supported USB3.0 device.

- Max 500mA at 5V
- Speed of operation: 1Mbps/12Mbps/480Mbps/5Gbps
- Storage only, not a data port

Note USBs with red/yellow port, for example the USBs with Sleep and Charge port, will not work on rommon prompt.



CHAPTER 2

Board-To-Board (BTB) Interface Connector

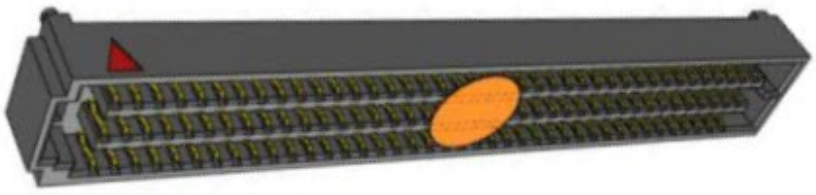
This chapter contains the following sections:

BTB Interface Connector Overview

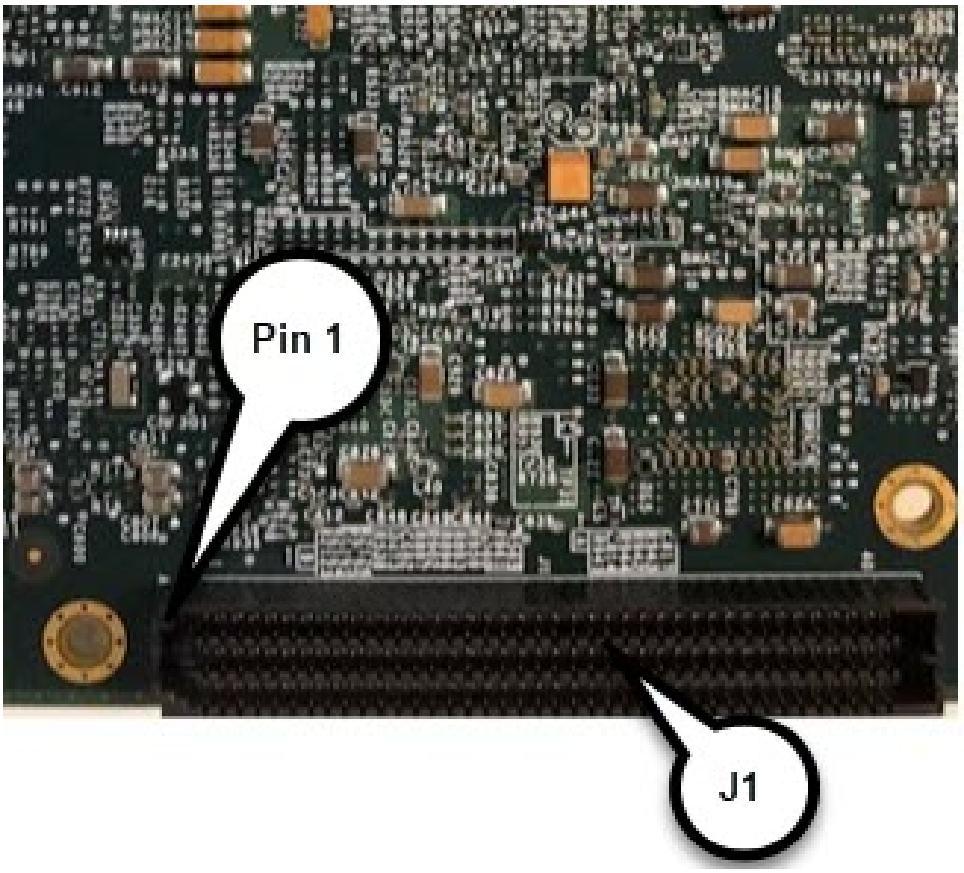
The board-to-board (BTB) connector provides the power input and the interface to external devices. This connector belongs to the SEARAY® Connector Series from SAMTEC. Depending on the mating connector selected by the integrator, the series supports a stacking height from 7mm to 18mm (not all increments are supported). The BTB connector on the ESR is the SAMTEC SEAF-40-05.0-S-06-2-A-K 240-pin female connector.

Complete information on the connector can be found at the Samtec website:

https://www.samtec.com/connectors/high-speed-board-to-board/high-density-arrays/searay



Note This figure is a partial view of the PCB to highlight the connector.



The following table lists the mating connector (SEAM lead style) options that are available to achieve specific stacking heights when coupled with the ESR (-05.0 SEAF lead style).

Mating Connector SEAM Lead Style	ESR Connector J1-05.0 SEAF Lead Style
-02.0	7mm
-03.0	8mm
-03.5	8.5mm
-05.5	N/A
-06.5	11.5mm
-07.0	12mm
-09.0	14mm

Mating Connector SEAM Lead Style	ESR Connector J1-05.0 SEAF Lead Style
-11.0	16mm
-13.0(not tooled)	18mm

ESR6300 Board-To-Board Connector (J1)

PIN #	Row A	Row B	Row C	Row D	Row E	Ro
1	+5V	+5V	+5V	+5V	+5V	+5
2	+5V	+5V	+5V	+5V	+5V	+5
3	GND	GND	GND	GND	GND	GN
4	GND	GND	GND	GND	GND	GN
5	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	RT
6	GND	GND	GND	GND	GND	GN
7	P4_MDI3_N	GND	P4_MDI2_N	GND	PCIE_REFCLK_P	P3
8	P4_MDI3_P	GND	P4_MDI2_P	GND	PCIE_REFCLK_N	GN
9	GND	P4_MDI1_N	GND	P4_MDI0_N	GND	AI
10	GND	P4_MDI1_P	GND	P4_MDI0_P	GND	PU
11	P3_MDI3_N	GND	P3_MDI2_N	GND	PIM_SGMII_RX_P	DC
12	P3_MDI3_P	GND	P3_MDI2_P	GND	PIM_SGMII_RX_N	PI
13	GND	P3_MDI1_N	GND	P3_MDI0_N	GND	US
14	GND	P3_MDI1_P	GND	P3_MDI0_P	GND	US
15	P2_MDI3_N	GND	P2_MDI2_N	GND	PIM_SGMII_TX_P	GN
16	P2_MDI3_P	GND	P2_MDI2_P	GND	PIM_SGMII_TX_N	CE
17	GND	P2_MDI1_N	GND	P2_MDI0_N	GND	CE
18	GND	P2_MDI1_P	GND	P2_MDI0_P	GND	CE
19	P1_MDI3_N	GND	P1_MDI2_N	GND	USBA_DP	CE
20	P1_MDI3_P	GND	P1_MDI2_P	GND	USBA_DN	GN
21	GND	P1_MDI1_N	GND	P1_MDI0_N	GND	CE

PIN #	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	P1_MDI1_P	GND	P1_MDI0_P	GND	CP_U
23	PIM_USB3_TX_N	GND	PIM_USB3_RX_P	GND	PIM_USB2_DP	R0_L
24	PIM_USB3_TX_P	GND	PIM_USB3_RX_N	GND	PIM_USB2_DN	R1_L
25	GND	USB3A_TX_N	GND	USB3A_RX_P	GND	C0_L
26	GND	USB3A_TX_P	GND	USB3A_RX_N	GND	C1_L
27	SSD_TX_SERDES_P	GND	SSD_RX_SERDES_P	GND	PIM_UA2_TXD	GND
28	SSD_TX_SERDES_N	GND	SSD_RX_SERDES_N	GND	PIM_UA2_RXD	P5_L
29	GND	SFP_2_TXD_P	GND	SFP_2_RXD_P	GND	SFP1_
30	GND	SFP_2_TXD_N	GND	SFP_2_RXD_N	GND	P6_L
31	P6_MDI3_N	GND	P6_MDI2_N	GND	PIM_GPS	SFP2_
32	P6_MDI3_P	GND	P6_MDI2_P	GND	ALM_LED_RED	GND
33	GND	P6_MDI1_P	GND	P6_MDI0_N	GND	AP_U
34	GND	P6_MDI1_N	GND	P6_MDI0_P	GND	AP_U
35	P5_MDI2_N	GND	P5_MDI1_N	GND	VPN_LED_GRN	GND
36	P5_MDI2_P	GND	P5_MDI1_P	GND	EVK_INT_L	I2C3_
37	GND	P5_MDI3_N	GND	P5_MDI0_P	GND	I2C3_
38	GND	P5_MDI3_P	GND	P5_MDI0_N	GND	GND
39	SFP_1_TXD_P	GND	SFP_1_RXD_P	GND	I2C2_SCL	SYS_
40	SFP_1_TXD_N	GND	SFP_1_RXD_N	+1.8V_OUT	I2C2_SDA	SYS_

Power and I/O Signals at the ESR BTB Connector

This section contains tables describing the control signals for different components. In the following tables, you will see the terms PU and PD. These stand for:

- PU = Pull-Up resistor
- PD = Pull-Down resistor

Note Differential pairs should be mostly routed on inner layers where the impedance tolerance is controlled better. Outer layers should only be used for very short differential pair traces (less than 0.25").

Power Signals

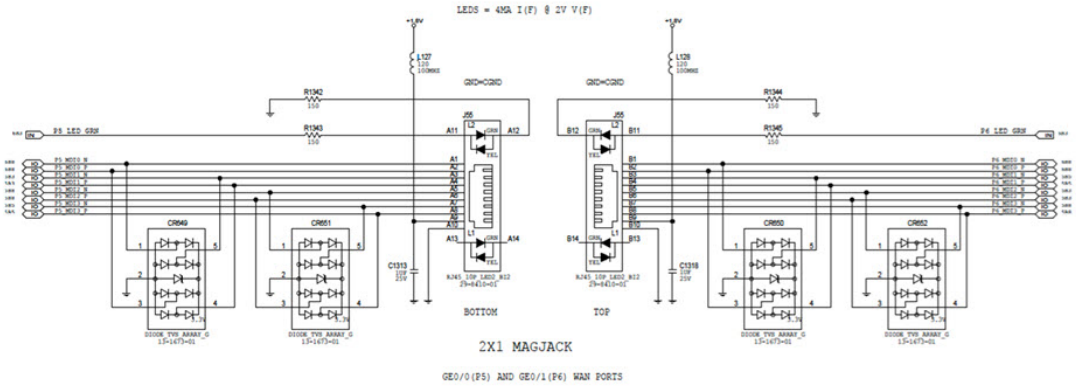
Signal Name	Direction	Terminations	Description	Levels
+5V	IN	—	+5V Power Input to ESR board	5V DC
+3.3V	IN	—	+3.3V Power Input to ESR board	3.3V DC
RTC_3.0V	IN	Series 1K resistor required at Host **Note 6**	+3.0V RTC Battery Power Input to ESR board	3.0V DC
GND	—	—	Ground	GND
+1.8V_OUT	OUT	—	+1.8V output from ESR board **Caution** 1.8V source is only intended for use as a WAN port center tap voltage as shown in the reference design schematic. 50mA is the max that can be drawn from that 1.8V output. See EVK Schematics below for further detail.	1.8V DC
P3V3_TRIM	—	—	Trim signal to margin 3.3V +/-5% See reference design schematic for proper usage. (For test purposes only. Leave unconnected if not used.)	Passive
DCIN_PWR_GOOD **Note 8**	IN	50K PU at ESR **Note 1**	External Power Supply Status Detect input (3.3V digital signal at the ESR connector). Can be used as an early power failure detect of the main power source. Active High (0 = Power Supply status is not good. 1 = Power Supply status is good.)	3.3V CMOS

Note 1: Signal driver can be open drain with a strong pullup (4.7K to 10K), or can be driven by 3.3V push-pull levels. A pull-down is not allowed on this signal. Can be left unconnected if not used.

Note 6: Series 1K current-limiting resistor is required on the host board for the RTC 3.0V battery.

Note 8: (currently not supported by software for graceful shutdown, but could be in the future). Used for successful CPU power up and boot. Must be driven or pulled high at powerup, or left open (because it is already pulled up by the ESR and keeps it in a “good” state for proper power up and CPU boot if left open).

Figure 7: EVK Schematic



LED Control Signals

Signal Name	Direction	Terminations	Description	Levels
SYS_LED_GRN_L	OUT	10K PD at ESR **Note 3** 270 Ohm series resistor at Host. **Note 7**	System Green LED Enable (active low)	3.3V CMOS
SYS_LED_YEL_L	OUT	10K PD at ESR **Note 3** 270 Ohm series resistor at Host. **Note 7**	System Yellow LED Enable (active low)	3.3V CMOS
ALM_LED_RED	OUT	1K PD at ESR **Note 3** 270 Ohm series resistor at Host. **Note 7**	Alarm Red LED Enable (active high)	3.3V CMOS
VPN_LED_GRN	OUT	4.7K PU at ESR **Note 3** 270 Ohm series resistor at Host. **Note 7**	VPN Green LED Enable (active high)	3.3V CMOS

Signal Name	Direction	Terminations	Description	Levels
R0_LED	OUT	270 Ohm series resistor at Host. **Note 7**	Row 0 LED control for LAN Ports GE 1/1 and GE 1/0. (controls cathode-side of 2 single-color LEDs). Cathode-side LED Enable (driven by Ethernet Switch on ESR) - Active Low. Tie to Cathode side of two single-color Green LEDs through a resistor to each (e.g., 270 ohms for a 5mA forward current on each of the 2 LEDs).	3.3V CMOS
C0_LED	OUT	4.7K PD at ESR **Note 3**	Column 0 LED control for LAN Ports GE 1/2 and GE 1/0. (controls anode-side of 2 single-color LEDs). (Anode-side LED Enable (driven by Ethernet Switch on ESR) - Active high. Tie **DIRECTLY** to Anode side of two single-color Green LEDs.	3.3V CMOS
R1_LED	OUT	270 Ohm series resistor at Host. **Note 7**	Row 1 LED control for LAN Ports **GE 1/3** and **GE 1/2**. (controls cathode-side of 2 single-color LEDs). Cathode-side LED Enable (driven by Ethernet Switch on ESR) - Active Low. Tie to Cathode side of two single-color Green LEDs through a resistor to each (for example, 270 ohms for a 5mA forward current on each of the 2 LEDs).	3.3V CMOS
C1_LED	OUT	4.7K PD at ESR **Note 3**	Column 1 LED control for LAN Ports **GE 1/3** and **GE 1/1**. (controls anode-side of 2 single-color LEDs). (Anode-side LED Enable (driven by Ethernet Switch on ESR) - Active high. Tie **DIRECTLY** to Anode side of two single-color Green LEDs.	3.3V CMOS
P5_LED_GRN	OUT	270 Ohm series resistor at Host. **Note 7**	WAN Copper Port (GE 0/0) LED Enable (controlled by Ethernet PHY on ESR) - Active High	3.3V CMOS
SFP1_LED_YEL	OUT	270 Ohm series resistor at Host. **Note 7**	WAN SFP Port (SFP 0/0) LED Enable (controlled by Ethernet PHY on ESR) - Active High	3.3V CMOS

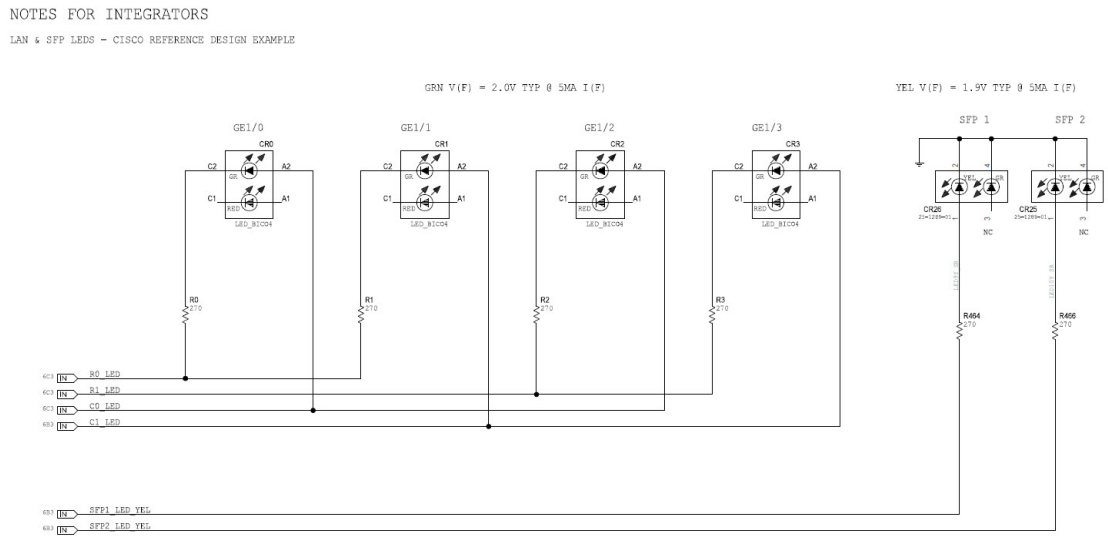
Signal Name	Direction	Terminations	Description	Levels
P6_LED_GRN	OUT	270 Ohm series resistor at Host. **Note 7**	WAN Copper Port (GE 0/1) LED Enable (controlled by Ethernet PHY on ESR) - Active High	3.3V CMOS
SFP2_LED_YEL	OUT	270 Ohm series resistor at Host. **Note 7**	WAN SFP Port (SFP 0/1) LED Enable (controlled by Ethernet PHY on ESR) - Active High	3.3V CMOS

Note 3: PU/PD to signals already exist on Cisco ESR, PIM, SFP, or SSD modules. No need to add any more. If you do add redundant parallel PU/PD, it should be weak (10K to 100K). Do not add a strong PU/PD for the purpose of overriding it to the opposite state. Some existing ESR PUs and PDs set the default configuration of the ESR CPU and should not be changed, as they are necessary during system reset to configure bootup settings. However, after any system reset (after system boots up), those signals are free to be driven and free to change states.

Note 7: Series current-limiting resistor is required on host board for the LED driving signals. LEDs on host board should be chosen so that they operate well at 5mA forward current.

See the following figure for a design reference.

Figure 8: LAN and SFP LED Reference Design



Note The Marvell Ethernet PHY chip set controls the LEDs, simply implement as shown in the reference design schematics. The Marvell chip minimizes the number of control lines by row and column to convey the correct link state and activity indication for all 4 ports. Cisco software does not control the ethernet port LEDs directly.

Gigabit Ethernet Port Signals

Signal Name	Direction	Terminations	Description	Levels	Impedance
SFP_2_TXD_[P/N]	OUT	Series Caps at SFP **Note 2**	Port 6 (WAN SFP 0/1) SFP Transmit Differential Pair	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
SFP_2_RXD_[P/N]	IN	Series Caps at SFP **Note 2**	Port 6 (WAN SFP 0/1) SFP Receive Differential Pair	2.1V Max LVDS	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
SFP_1_TXD_[P/N]	OUT	Series Caps at SFP **Note 2**	Port 5 (WAN SFP 0/0) SFP Transmit Differential Pair	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
SFP_1_RXD_[P/N]	IN	Series Caps at SFP **Note 2**	Port 5 (WAN SFP 0/0) SFP Receive Differential Pair	2.1V Max LVDS	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P6_MDI[3..0]_[P/N]	BI	—	Port 6 (WAN GE 0/1) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	2.8V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P5_MDI[3..0]_[P/N]	BI	—	Port 5 (WAN GE 0/0) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	2.8V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P4_MDI[3..0]_[P/N]	BI	—	Port 4 (LAN GE 1/3) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	1.4V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P3_MDI[3..0]_[P/N]	BI	—	Port 3 (LAN GE 1/2) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	1.4V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P2_MDI[3..0]_[P/N]	BI	—	Port 2 (LAN GE 1/1) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	1.4V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P1_MDI[3..0]_[P/N]	BI	—	Port 1 (LAN GE 1/0) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	1.4V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers

Note 2: Series AC-coupling caps to SERDES signals already exist on Cisco ESR, PIM or SFP module. No need to add any more.

Module Interface Signals

Signal Name	Direction	Terminations	Description	Levels	Impedance
PCIE_REFCLK_[P/N]	OUT	If not used, keep open. The router will disable the PCIE reference clock when no PCIe is present.	PCIe 100MHz Differential Pair Reference Clock for Pluggable or SSD Module	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_SGMII_TX_[P/N]	OUT	Series Caps at PIM **Note 2**	SGMII Transmit Differential Pair for Pluggable Module (Can be PCIe TX also)	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_SGMII_RX_[P/N]	IN	Series Caps at ESR **Note 2**	SGMII Receive Differential Pair for Pluggable Module (Can be PCIe RX also)	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_USB3_TX_[P/N]	OUT	Series Caps at ESR **Note 2**	USB 3.0 Transmit Differential Pair for Pluggable Module	1.2V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_USB3_RX_[P/N]	IN	Series Caps at PIM **Note 2**	USB 3.0 Receive Differential Pair for Pluggable Module	1.2V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_USB2_[DP/DN]	BI	2x 15K PD at ESR	USB 2.0 Differential Pair for Pluggable Module	3.6V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_UA2_TXD	OUT	10K PU at PIM **Note 3**	UART2 Transmit Data for Pluggable Module	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +-15% (outer layers
PIM_UA2_RXD	IN	4.7K PU at ESR **Note 3**	UART2 Receive Data for Pluggable Module	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +-15% (outer layers
SSD_TX_SERDES_[P/N]	OUT	Series Caps at Host **Note 4**	SERDES Transmit Differential Pair for SSD Module (Can be SATA or PCIe)	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +-15% (outer layers

Signal Name	Direction	Terminations	Description	Levels	Impedance
SSD_RX_SERDES_[P/N]	IN	Series Caps at ESR **Note 2**	SERDES Receive Differential Pair for SSD Module (Can be SATA or PCIe)	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_PWR_EN	OUT	1K PD at PIM **Note 3**	Power Enable signal for the Pluggable Module. Active high (0 = disable Pluggable power. 1 = Enable Pluggable power.)	3.3V CMOS	—
PIM_GPS	IN	4.7K PU at ESRIf not used, keep open. The router will pull it up and keep it in an idle state. **Note 3**	GPS Pulse Per Second Timing signal from Pluggable Module	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +-15% (outer layers

Note 2: Series AC-coupling caps to SERDES signals already exist on Cisco ESR, PIM or SFP module. No need to add any more.

Note 3: PU/PD to signals already exist on Cisco ESR, PIM, SFP, or SSD modules. No need to add any more. If you do add redundant parallel PU/PD, it should be weak (10K to 100K). Do not add a strong PU/PD for the purpose of overriding it to the opposite state. Some existing ESR PUs and PDs set the default configuration of the ESR CPU and should not be changed.

Note 4: Series caps required on the host board for these SERDES signals.

External Port Signals

Signal Name	Direction	Terminations	Description	Levels	Impedance
USB3A_TX_[P/N]	OUT	Series Caps at ESR **Note 2**	USB 3.0 Transmit Differential Pair for External USB Host Port	1.2V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers
USB3A_RX_[P/N]	IN	Series Caps at Host **Note 4**	USB 3.0 Receive Differential Pair for External USB Host Port	1.2V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers
USBA_[DP/DN]	BI	2x 15K PD at ESR	USB 2.0 Differential Pair for External USB Host Port	3.6V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers

Signal Name	Direction	Terminations	Description	Levels	Impedance
USBA_5V_EN	OUT	1K PD at ESR **Note 3**	Enable 5V output of the external USB Host Port. Active High (0 = disable 5V USB output. 1 = enable USB 5V output)	3.3V CMOS	—
USBA_OC_L	IN	10K PU at Host **Note 5**	Over Current Detect of the external USB Host Port. Active Low (0 = USB host port 5V is in overcurrent condition. 1 = Normal Operation)	3.3V CMOS	—
CP_UA0_DTR	OUT	10K PU at Host **Note 5**	UART0 DTR flow control signal for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
CP_UA0_DSR	IN	4.7K PU at ESR **Note 3**	UART0 DSR flow control signal for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
CP_UA0_RTS	OUT	10K PU at Host **Note 5**	UART0 RTS flow control signal for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
CP_UA0_CTS	IN	4.7K PU at ESR **Note 3**	UART0 CTS flow control signal for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
CP_UA0_TXD	OUT	10K PU at Host **Note 5**	UART0 Transmit Data for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
CP_UA0_RXD	IN	4.7K PU at ESR **Note 3**	UART0 Receive Data for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
AP_UA0_TXD	OUT	1K PD at ESR **Note 3**	Transmit Data for Console Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
AP_UA0_RXD	IN	100K PU at Host **Note 5**	Receive Data for Console Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers

Signal Name	Direction	Terminations	Description	Levels	Impedance
ALM_IN_L	IN	4.7K PU at ESRIf not used, keep open. The router will pull it up and keep it in an idle state. **Note 3**	Alarm Input (3.3V digital signal at the ESR connector). Active Low (0 = external alarm port is closed. 1 = external alarm port is open circuit)	3.3V CMOS	—
PUSHBUTTON_L	IN	4.7K PU at ESRIf not used, keep open. The router will pull it up and keep it in an idle state. **Note 3**	Pushbutton Detect Input (3.3V digital signal at the ESR connector). Active Low (0 = pushbutton is closed. 1 = pushbutton is open).	3.3V CMOS	—

Note 2: Series AC-coupling caps to SERDES signals already exist on Cisco ESR, PIM or SFP module. No need to add any more.

Note 3: PU/PD to signals already exist on Cisco ESR, PIM, SFP, or SSD modules. No need to add any more. If you do add redundant parallel PU/PD, it should be weak (10K to 100K). Do not add a strong PU/PD for the purpose of overriding it to the opposite state. Some existing ESR PUs and PDs set the default configuration of the ESR CPU and should not be changed.

Note 4: Series caps required on the host board for these SERDES signals.

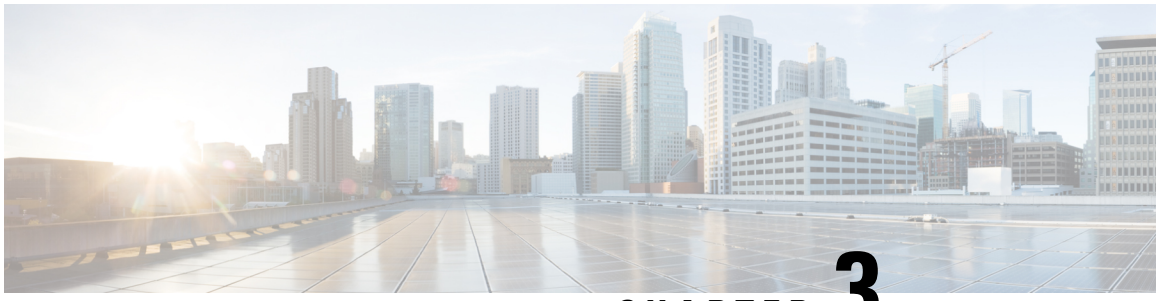
Note 5: PU/PD are required on the host board for these signals.

Miscellaneous Control Signals

Signal Name	Direction	Terminations	Description	Levels	Impedance
EVK_INT_L	IN	4.7K PU at ESR **Note 3**	Reserved for Interrupt input to the ESR CPU from the host board. Currently not used by the Cisco Software to detect interrupts from the host motherboard. User should leave this signal unconnected, as the ESR provides the pullup.	3.3V CMOS	—
I2C2_SCL	OUT	4.7K PU at ESR **Note 3**	Output Clock for I2C bus #2 to host board	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
I2C2_SDA	BI	4.7K PU at ESR **Note 3**	Bidirectional Data for I2C bus #2 to host board	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
I2C3_SCL	OUT	4.7K PU at ESR **Note 3**	Output Clock for I2C bus #3 to host board	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers

Signal Name	Direction	Terminations	Description	Levels	Impedance
I2C3_SDA	BI	4.7K PU at ESR **Note 3**	Bidirectional Data for I2C bus #3 to host board	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers

Note 3: PU/PD to signals already exist on Cisco ESR, PIM, SFP, or SSD modules. No need to add any more. If you do add redundant parallel PU/PD, it should be weak (10K to 100K). Do not add a strong PU/PD for the purpose of overriding it to the opposite state. Some existing ESR PUs and PDs set the default configuration of the ESR CPU and should not be changed.



CHAPTER 3

Power and I/O Signals at the ESR BTB Connector

This chapter contains the following sections:

Power and I/O Signals at the ESR BTB Connector

This section contains tables describing the control signals for different components. In the following tables, you will see the terms PU and PD. These stand for:

- PU = Pull-Up resistor
- PD = Pull-Down resistor

Note Differential pairs should be mostly routed on inner layers where the impedance tolerance is controlled better. Outer layers should only be used for very short differential pair traces (less than 0.25").

Power Signals

Signal Name	Direction	Terminations	Description	Levels
+5V	IN	—	+5V Power Input to ESR board	5V DC
+3.3V	IN	—	+3.3V Power Input to ESR board	3.3V DC
RTC_3.0V	IN	Series 1K resistor required at Host **Note 6**	+3.0V RTC Battery Power Input to ESR board	3.0V DC

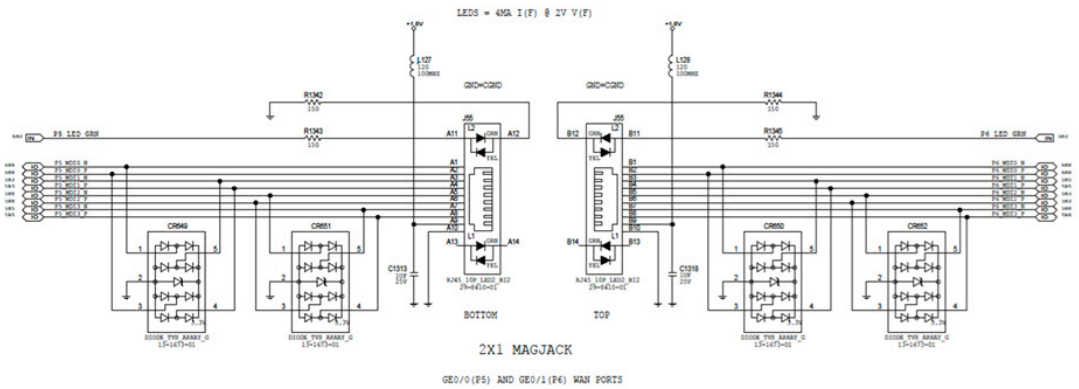
Signal Name	Direction	Terminations	Description	Levels
GND	—	—	Ground	GND
+1.8V_OUT	OUT	—	+1.8V output from ESR board **Caution** 1.8V source is only intended for use as a WAN port center tap voltage as shown in the reference design schematic. 50mA is the max that can be drawn from that 1.8V output. See EVK Schematics below for further detail.	1.8V DC
P3V3_TRIM	—	—	Trim signal to margin 3.3V +/-5% See reference design schematic for proper usage. (For test purposes only. Leave unconnected if not used.)	Passive
DCIN_PWR_GOOD **Note 8**	IN	50K PU at ESR **Note 1**	External Power Supply Status Detect input (3.3V digital signal at the ESR connector). Can be used as an early power failure detect of the main power source. Active High (0 = Power Supply status is not good. 1 = Power Supply status is good.)	3.3V CMOS

Note 1: Signal driver can be open drain with a strong pullup (4.7K to 10K), or can be driven by 3.3V push-pull levels. A pull-down is not allowed on this signal. Can be left unconnected if not used.

Note 6: Series 1K current-limiting resistor is required on the host board for the RTC 3.0V battery.

Note 8: (currently not supported by software for graceful shutdown, but could be in the future). Used for successful CPU power up and boot. Must be driven or pulled high at powerup, or left open (because it is already pulled up by the ESR and keeps it in a “good” state for proper power up and CPU boot if left open).

Figure 9: EVK Schematic



LED Control Signals

Signal Name	Direction	Terminations	Description	Levels
SYS_LED_GRN_L	OUT	10K PD at ESR **Note 3** 270 Ohm series resistor at Host. **Note 7**	System Green LED Enable (active low)	3.3V CMOS
SYS_LED_YEL_L	OUT	10K PD at ESR **Note 3** 270 Ohm series resistor at Host. **Note 7**	System Yellow LED Enable (active low)	3.3V CMOS
ALM_LED_RED	OUT	1K PD at ESR **Note 3** 270 Ohm series resistor at Host. **Note 7**	Alarm Red LED Enable (active high)	3.3V CMOS
VPN_LED_GRN	OUT	4.7K PU at ESR **Note 3** 270 Ohm series resistor at Host. **Note 7**	VPN Green LED Enable (active high)	3.3V CMOS
R0_LED	OUT	270 Ohm series resistor at Host. **Note 7**	Row 0 LED control for LAN Ports GE 1/1 and GE 1/0. (controls cathode-side of 2 single-color LEDs). Cathode-side LED Enable (driven by Ethernet Switch on ESR) - Active Low. Tie to Cathode side of two single-color Green LEDs through a resistor to each (e.g., 270 ohms for a 5mA forward current on each of the 2 LEDs).	3.3V CMOS

Signal Name	Direction	Terminations	Description	Levels
C0_LED	OUT	4.7K PD at ESR **Note 3**	Column 0 LED control for LAN Ports GE 1/2 and GE 1/0. (controls anode-side of 2 single-color LEDs). (Anode-side LED Enable (driven by Ethernet Switch on ESR) - Active high. Tie **DIRECTLY** to Anode side of two single-color Green LEDs.	3.3V CMOS
R1_LED	OUT	270 Ohm series resistor at Host. **Note 7**	Row 1 LED control for LAN Ports **GE 1/3** and **GE 1/2**. (controls cathode-side of 2 single-color LEDs). Cathode-side LED Enable (driven by Ethernet Switch on ESR) - Active Low. Tie to Cathode side of two single-color Green LEDs through a resistor to each (for example, 270 ohms for a 5mA forward current on each of the 2 LEDs).	3.3V CMOS
C1_LED	OUT	4.7K PD at ESR **Note 3**	Column 1 LED control for LAN Ports **GE 1/3** and **GE 1/1**. (controls anode-side of 2 single-color LEDs). (Anode-side LED Enable (driven by Ethernet Switch on ESR) - Active high. Tie **DIRECTLY** to Anode side of two single-color Green LEDs.	3.3V CMOS
P5_LED_GRN	OUT	270 Ohm series resistor at Host. **Note 7**	WAN Copper Port (GE 0/0) LED Enable (controlled by Ethernet PHY on ESR) - Active High	3.3V CMOS
SFP1_LED_YEL	OUT	270 Ohm series resistor at Host. **Note 7**	WAN SFP Port (SFP 0/0) LED Enable (controlled by Ethernet PHY on ESR) - Active High	3.3V CMOS
P6_LED_GRN	OUT	270 Ohm series resistor at Host. **Note 7**	WAN Copper Port (GE 0/1) LED Enable (controlled by Ethernet PHY on ESR) - Active High	3.3V CMOS
SFP2_LED_YEL	OUT	270 Ohm series resistor at Host. **Note 7**	WAN SFP Port (SFP 0/1) LED Enable (controlled by Ethernet PHY on ESR) - Active High	3.3V CMOS

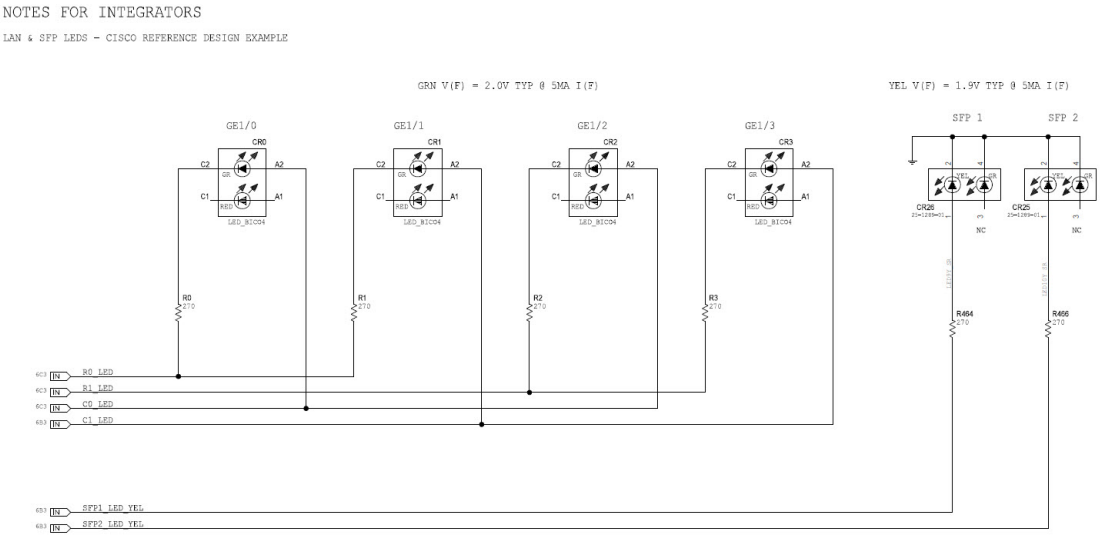
Note 3: PU/PD to signals already exist on Cisco ESR, PIM, SFP, or SSD modules. No need to add any more. If you do add redundant parallel PU/PD, it should be weak (10K to 100K). Do not add a strong PU/PD for the purpose of overriding it to the opposite state. Some existing ESR PUs and PDs set the default configuration

of the ESR CPU and should not be changed, as they are necessary during system reset to configure bootup settings. However, after any system reset (after system boots up), those signals are free to be driven and free to change states.

Note 7: Series current-limiting resistor is required on host board for the LED driving signals. LEDs on host board should be chosen so that they operate well at 5mA forward current.

See the following figure for a design reference.

Figure 10: LAN and SFP LED Reference Design



Note The Marvell Ethernet PHY chip set controls the LEDs, simply implement as shown in the reference design schematics. The Marvell chip minimizes the number of control lines by row and column to convey the correct link state and activity indication for all 4 ports. Cisco software does not control the ethernet port LEDs directly.

Gigabit Ethernet Port Signals

Signal Name	Direction	Terminations	Description	Levels	Impedance
SFP_2_TXD_[P/N]	OUT	Series Caps at SFP **Note 2**	Port 6 (WAN SFP 0/1) SFP Transmit Differential Pair	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
SFP_2_RXD_[P/N]	IN	Series Caps at SFP **Note 2**	Port 6 (WAN SFP 0/1) SFP Receive Differential Pair	2.1V Max LVDS	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers

Signal Name	Direction	Terminations	Description	Levels	Impedance
SFP_1_TXD_[P/N]	OUT	Series Caps at SFP **Note 2**	Port 5 (WAN SFP 0/0) SFP Transmit Differential Pair	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
SFP_1_RXD_[P/N]	IN	Series Caps at SFP **Note 2**	Port 5 (WAN SFP 0/0) SFP Receive Differential Pair	2.1V Max LVDS	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P6_MDI[3..0]_[P/N]	BI	—	Port 6 (WAN GE 0/1) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	2.8V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P5_MDI[3..0]_[P/N]	BI	—	Port 5 (WAN GE 0/0) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	2.8V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P4_MDI[3..0]_[P/N]	BI	—	Port 4 (LAN GE 1/3) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	1.4V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P3_MDI[3..0]_[P/N]	BI	—	Port 3 (LAN GE 1/2) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	1.4V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P2_MDI[3..0]_[P/N]	BI	—	Port 2 (LAN GE 1/1) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	1.4V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers
P1_MDI[3..0]_[P/N]	BI	—	Port 1 (LAN GE 1/0) MDI Differential Pairs for 10/100/1000 Gigabit Ethernet Copper Ports	1.4V Max MDI	100 Ohm Differential +/-10% (inner layers) +/-15% (outer layers

Note 2: Series AC-coupling caps to SERDES signals already exist on Cisco ESR, PIM or SFP module. No need to add any more.

Module Interface Signals

Signal Name	Direction	Terminations	Description	Levels	Impedance
PCIE_REFCLK_[P/N]	OUT	If not used, keep open. The router will disable the PCIE reference clock when no PCIe is present.	PCIe 100MHz Differential Pair Reference Clock for Pluggable or SSD Module	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_SGMII_TX_[P/N]	OUT	Series Caps at PIM **Note 2**	SGMII Transmit Differential Pair for Pluggable Module (Can be PCIe TX also)	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_SGMII_RX_[P/N]	IN	Series Caps at ESR **Note 2**	SGMII Receive Differential Pair for Pluggable Module (Can be PCIe RX also)	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_USB3_TX_[P/N]	OUT	Series Caps at ESR **Note 2**	USB 3.0 Transmit Differential Pair for Pluggable Module	1.2V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_USB3_RX_[P/N]	IN	Series Caps at PIM **Note 2**	USB 3.0 Receive Differential Pair for Pluggable Module	1.2V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_USB2_[DP/DN]	BI	2x 15K PD at ESR	USB 2.0 Differential Pair for Pluggable Module	3.6V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_UA2_TXD	OUT	10K PU at PIM **Note 3**	UART2 Transmit Data for Pluggable Module	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +-15% (outer layers
PIM_UA2_RXD	IN	4.7K PU at ESR **Note 3**	UART2 Receive Data for Pluggable Module	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +-15% (outer layers
SSD_TX_SERDES_[P/N]	OUT	Series Caps at Host **Note 4**	SERDES Transmit Differential Pair for SSD Module (Can be SATA or PCIe)	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +-15% (outer layers

Signal Name	Direction	Terminations	Description	Levels	Impedance
SSD_RX_SERDES_[P/N]	IN	Series Caps at ESR **Note 2**	SERDES Receive Differential Pair for SSD Module (Can be SATA or PCIe)	1.6V Max LVDS	100 Ohm Differential +/-10% (inner layers) +-15% (outer layers
PIM_PWR_EN	OUT	1K PD at PIM **Note 3**	Power Enable signal for the Pluggable Module. Active high (0 = disable Pluggable power. 1 = Enable Pluggable power.)	3.3V CMOS	—
PIM_GPS	IN	4.7K PU at ESRIf not used, keep open. The router will pull it up and keep it in an idle state. **Note 3**	GPS Pulse Per Second Timing signal from Pluggable Module	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +-15% (outer layers

Note 2: Series AC-coupling caps to SERDES signals already exist on Cisco ESR, PIM or SFP module. No need to add any more.

Note 3: PU/PD to signals already exist on Cisco ESR, PIM, SFP, or SSD modules. No need to add any more. If you do add redundant parallel PU/PD, it should be weak (10K to 100K). Do not add a strong PU/PD for the purpose of overriding it to the opposite state. Some existing ESR PUs and PDs set the default configuration of the ESR CPU and should not be changed.

Note 4: Series caps required on the host board for these SERDES signals.

External Port Signals

Signal Name	Direction	Terminations	Description	Levels	Impedance
USB3A_TX_[P/N]	OUT	Series Caps at ESR **Note 2**	USB 3.0 Transmit Differential Pair for External USB Host Port	1.2V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers
USB3A_RX_[P/N]	IN	Series Caps at Host **Note 4**	USB 3.0 Receive Differential Pair for External USB Host Port	1.2V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers
USBA_[DP/DN]	BI	2x 15K PD at ESR	USB 2.0 Differential Pair for External USB Host Port	3.6V Max USB	90 Ohm Differential +/-10% (inner layers) +-15% (outer layers

Signal Name	Direction	Terminations	Description	Levels	Impedance
USBA_5V_EN	OUT	1K PD at ESR **Note 3**	Enable 5V output of the external USB Host Port. Active High (0 = disable 5V USB output. 1 = enable USB 5V output)	3.3V CMOS	—
USBA_OC_L	IN	10K PU at Host **Note 5**	Over Current Detect of the external USB Host Port. Active Low (0 = USB host port 5V is in overcurrent condition. 1 = Normal Operation)	3.3V CMOS	—
CP_UA0_DTR	OUT	10K PU at Host **Note 5**	UART0 DTR flow control signal for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
CP_UA0_DSR	IN	4.7K PU at ESR **Note 3**	UART0 DSR flow control signal for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
CP_UA0_RTS	OUT	10K PU at Host **Note 5**	UART0 RTS flow control signal for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
CP_UA0_CTS	IN	4.7K PU at ESR **Note 3**	UART0 CTS flow control signal for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
CP_UA0_TXD	OUT	10K PU at Host **Note 5**	UART0 Transmit Data for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
CP_UA0_RXD	IN	4.7K PU at ESR **Note 3**	UART0 Receive Data for external RS232 Serial Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
AP_UA0_TXD	OUT	1K PD at ESR **Note 3**	Transmit Data for Console Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
AP_UA0_RXD	IN	100K PU at Host **Note 5**	Receive Data for Console Port	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers

Signal Name	Direction	Terminations	Description	Levels	Impedance
ALM_IN_L	IN	4.7K PU at ESRIf not used, keep open. The router will pull it up and keep it in an idle state. **Note 3**	Alarm Input (3.3V digital signal at the ESR connector). Active Low (0 = external alarm port is closed. 1 = external alarm port is open circuit)	3.3V CMOS	—
PUSHBUTTON_L	IN	4.7K PU at ESRIf not used, keep open. The router will pull it up and keep it in an idle state. **Note 3**	Pushbutton Detect Input (3.3V digital signal at the ESR connector). Active Low (0 = pushbutton is closed. 1 = pushbutton is open).	3.3V CMOS	—

Note 2: Series AC-coupling caps to SERDES signals already exist on Cisco ESR, PIM or SFP module. No need to add any more.

Note 3: PU/PD to signals already exist on Cisco ESR, PIM, SFP, or SSD modules. No need to add any more. If you do add redundant parallel PU/PD, it should be weak (10K to 100K). Do not add a strong PU/PD for the purpose of overriding it to the opposite state. Some existing ESR PUs and PDs set the default configuration of the ESR CPU and should not be changed.

Note 4: Series caps required on the host board for these SERDES signals.

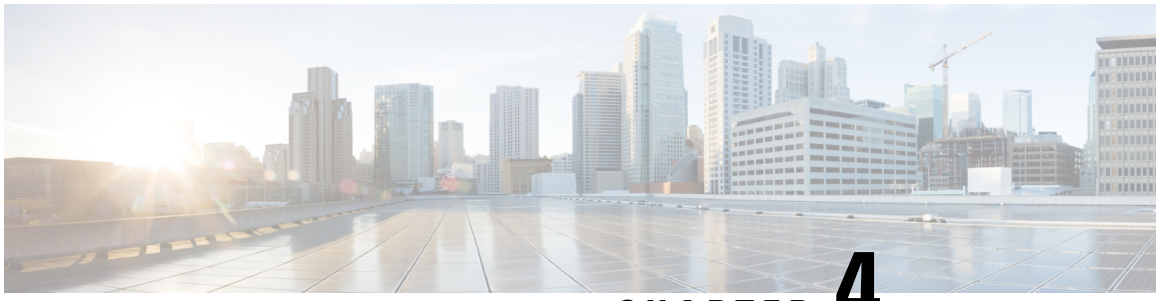
Note 5: PU/PD are required on the host board for these signals.

Miscellaneous Control Signals

Signal Name	Direction	Terminations	Description	Levels	Impedance
EVK_INT_L	IN	4.7K PU at ESR **Note 3**	Reserved for Interrupt input to the ESR CPU from the host board. Currently not used by the Cisco Software to detect interrupts from the host motherboard. User should leave this signal unconnected, as the ESR provides the pullup.	3.3V CMOS	—
I2C2_SCL	OUT	4.7K PU at ESR **Note 3**	Output Clock for I2C bus #2 to host board	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
I2C2_SDA	BI	4.7K PU at ESR **Note 3**	Bidirectional Data for I2C bus #2 to host board	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers
I2C3_SCL	OUT	4.7K PU at ESR **Note 3**	Output Clock for I2C bus #3 to host board	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers

Signal Name	Direction	Terminations	Description	Levels	Impedance
I2C3_SDA	BI	4.7K PU at ESR **Note 3**	Bidirectional Data for I2C bus #3 to host board	3.3V CMOS	50 Ohm Single-Ended +/-10% (inner layers) +/-15% (outer layers

Note 3: PU/PD to signals already exist on Cisco ESR, PIM, SFP, or SSD modules. No need to add any more. If you do add redundant parallel PU/PD, it should be weak (10K to 100K). Do not add a strong PU/PD for the purpose of overriding it to the opposite state. Some existing ESR PUs and PDs set the default configuration of the ESR CPU and should not be changed.



CHAPTER 4

Implementation Options

This chapter contains the following sections:

Thermal Design Considerations

The following sections outline the methods for dealing with thermal issues and the mounting options involving the Cisco-designed conduction cooling plate.

As the Cisco ESR6300 is intended for use in extreme environments, industrial temperature rated components are used. The SKUs with a thermal plate make integration easier by abstracting the component level thermal concerns. Cisco has already performed the thermal analysis at the component level so that the integrator need only be concerned with the thermal plate temperature. As a general rule, the thermal plate of the card needs to make contact with an adequate thermal mass to draw heat away from the card. This can be done in a number of ways.

The important note is that the thermal plate temperature, as measured at the center of the top surface of the thermal plate, must not exceed 85° C. As long as this requirement is satisfied, all of the card's components will be within a safe operating temperature range on the high temperature side.

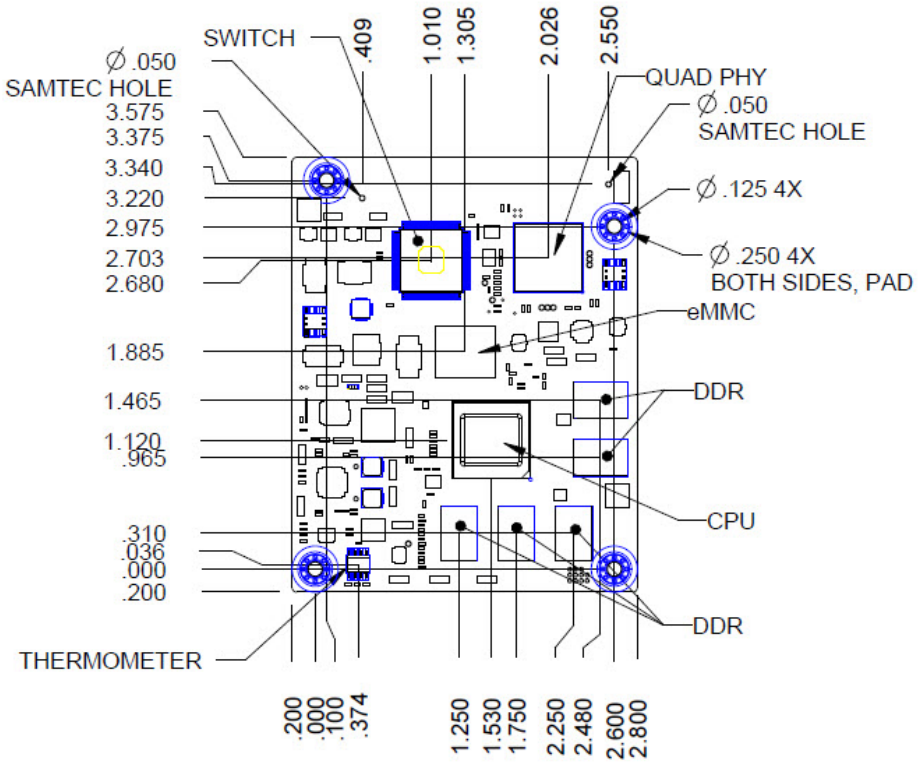
Heat dissipation methods:

As a general rule, the thermal plate of the board needs to make contact with an adequate thermal mass to draw heat away from the board. There are many ways to achieve this goal.

Examples:

- Transfer heat away from the thermal plate and into the enclosure wall by utilizing a “shelf” of metal. The shelf encompasses the entire Cisco ESR6300 thermal plate surface. This shelf is illustrated by item 1 in the following figure.
- Mount the Cisco ESR6300 thermal plate directly to the enclosure wall by using thermal interface material.

Figure 11: Thermally Significant Components of Cisco ESR6300 Board



RefDes	Part Type	Thermal Design Power (W)	Allowable Junction Temperature	Allowable Case Temperature	Package Type	Theta JC (degC/W)	Theta JB (degC/W)
U83	Quad Phy	1.5	125	—	TFBGA196	7.9	23.5
U45	Switch	2.5	125	—	TQFP128	7.7	15.5
U16	eMMC	1.0	—	90	FBGA153	—	—
U47	CPU	9.3	105	—	TFBGA430	0.6	4.3
U25U26U27U72U73	DDR	0.2 each	—	95	FPGA96	3.0	—
U2401	Temperature Sensor	—	125	—	MSOP8	—	—

Validating a Thermal Solution

To validate a thermal solution, monitor the thermal sensor of the Cisco ESR6300 cards in a thermal chamber set to the desired maximum ambient operating temperature and with traffic running.

Each card has a single sensor located on the corner of the card, which makes contact with the thermal plate using thermal interface material. The temperature of the sensors should be less than 90.5C. The **show environment all** command can be executed from the IOS prompt to monitor the thermal sensor temperatures

```
router# show environment all
ALARM CONTACT 1
   Status:      not asserted
   Description: external alarm contact 1
   Severity:    minor
   Trigger:     closed
ALARM CONTACT 2
   Status:      not asserted
   Description: external alarm contact 2
   Severity:    minor
   Trigger:     closed
Supervisor Temperature Value: 51 C
Temperature State: GREEN
System Temperature thresholds
---------------------------------
Minor Threshold    : 80 C (Yellow)
Major Threshold    : 90 C (Red)
Critical Threshold : 96 C
Shutdown Threshold : 105 C
Pwr Supply         Type     Status
------------------------------------
POWER SUPPLY-A      DC      OK
POWER SUPPLY-B      DC      OK
 SYSTEM TEMPERATURE is OK
 System Temperature Value: 36 Degree Celsius
 Extension Board Temperature Value: 32 Degree Celsius
```

Product Specifications

The following table lists the product specifications for the Cisco ESR6300.

Table 1: Memory

DRAM	4GB
SPI Flash	16MB for the rommon (boot loader)
eMMC Flash	4GB (in pSLC mode) for Cisco IOS

Table 2: Environmental

Industrial-grade components	-40F to +185F (-40C to +85C) component local ambient temperature specifications

Operating temperature	Temperature range of a completed solution depends on the enclosure thermal design characteristics used by the integrator. If –NCP SKU is used, integrator is responsible for designing a thermal solution that meets the component level requirements provided in this document.
Non-Operating Temperature	-40F to +185F (-40C to +85C)
Operating altitude	15,000ft (4,572m)
Non-operating altitude	40,000ft (12,200m)
Humidity	95% +/- 5% RH

Table 3: Hardware

Input voltages	+5Vdc (+/- 5%) and +3.3Vdc (+/- 3%)
Total Power Consumption	5.0W typical at idle, at +77F (+25C) 9.6W typical with full traffic, at +158F (+70C) 12W measured maximum
Mass	ESR-6300-NCP-K9: 41 grams ESR-6300-CON-K9: 212 grams
Mean Time Before Failure	ESR-6300 (-CON and –NCP) standalone. Ground, Fixed, Controlled: 1,065,092 (in hours)

Power Requirements

The ESR6300 requires +5 VDC and +3.3 VDC to operate. The following table lists the DC power requirements.

Note There are no timing or sequencing requirements for the power input.

Voltage Rail	Tolerance	Typical Current (A)	Maximum Current (A)
5V	+/- 5%	N/A	2.2
3.3V	+/- 3%	N/A	0.5
P3_3V RTC	+10% / -60%	400e-9	700e-9

Power Over Ethernet (PoE)

The ESR6300 supports IOS software control of PoE if the partner adds the appropriate circuitry to their host chassis. A maximum of 120W of power is supported through to PDs via the per port PSE controllers.

Note The actual amount of power available for POE may be less depending on size of the power supply included by the integrator.

The integrator should contact Cisco for any additional details.

SFP Support

Both 100BASE-X and 1000BASE-X SFP transceivers are supported by the router.

Supported 1000M SFP Modules

SFP	Distance	Fiber	Commercial(0C to 70C)	Extended(-5C to 85C)	Industrial(-40C to 85C)	DOM
GLC-SX-MM-RGD	220-550 m	MMF	—	—	X	
GLC-LX-SM-RGD	550 m/10 km	MMF/SMF	—	—	X	X
GLC-ZX-SM-RGD	70 km	SMF	—	—	X	X
GLC-SX-MMD	220-550 m	MMF	—	X	—	X
GLC-LH-SMD	550 m/10 km	MMF/SMF	—	X	—	X
GLC-ZX-SMD	70km	SMF	—	X	—	X
GLC-LH-MMD	550 m/10 km	MMF/SMF	—	X	—	X
GLC-BX-U	10 km	SMF	X	—	—	X
GLC-BX-D	10 km	SMF	X	—	—	X
GLC-EX-SMD	40 km	SMF	—	X	—	X
GLC-T-RGD	100 m	N/A	—	—	X	
GLC-T, GLC-TE (see note below)	100 m	N/A	X	—	—	

Note The GLC-T and GLC-TE are the only copper SFPs supported by Cisco, and the **service unsupported-transceiver** CLI must be added if they are used.

Supported 100M Fast Ethernet SFP Modules

SFP	Distance	Fiber	Commercial(0C to 70C)	Extended(-5C to 85C)	Industrial(-40C to 85C)	DOM
GLC-FE-100FX-RGD	2 km	MMF	—	—	X	
GLC-FE-100LX-RGD	10 km	SMF	—	—	X	
GLC-FE-100FX	2 km	MMF	X	—	—	
GLC-FE-100LX	10 km	SMF	X	—	—	
GLC-FE-100EX	40 km	SMF	X	—	—	
GLC-FE-100ZX	80 km	SMF	X	—	—	
GLC-FE-100BX-U	10 km	SMF	X	—	—	
GLC-FE-100BX-D	10 km	SMF	X	—	—	

Note The following CLIs are used to show the output for DOM features:

```
Router#sh hw-module subslot 0/0 transceiver 0 status
Router#sh hw-module subslot 0/0 transceiver 0 idprom detail
```

The subslot comes from the first two digits in the interface name, and the transceiver port number comes from the last digit.

SFPs Supported in IOS XE 17.7.1

The following SFPs are supported in IOS XE release 17.7.1:

Table 4: Supported SFPs added in IOS XE 17.7.1

SFP	Distance	Fiber	Commercial 0C ~ +70C	Extended -5C ~ +85C	Industrial -40C ~ +85C	DOM
GLC-T-RGD	100 M	Copper			YES	
CWDM-SFP-1470	100 km	Duplex	YES			YES

SFP	Distance	Fiber	Commercial 0C ~ +70C	Extended -5C ~ +85C	Industrial -40C ~ +85C	DOM
CWDM-SFP-1610	100 km	Duplex	YES			YES
CWDM-SFP-1530	100 km	Duplex	YES			YES
DWDM-SFP-3033	80 km	Duplex	YES			YES
DWDM-SFP-3112	80 km	Duplex	YES			YES
GLC-BX-D-I	10 km	Single Strand			YES	YES
GLC-BX-U-I	10 km	Single Strand			YES	YES
GLC-TE	100 km	Copper			YES	NO

LED Definitions

Eight LEDs are available for general use. Six of these are already defined and two are reserved for use by the integrator. See the following table.

LED	Color	Description
System (SYS)	Off Flashing Green Green Flashing Yellow Yellow	No Power Boot up phase Normal Operation Zeroization Process started Power is OK but possible internal failure
Power (PWR)	Off Green Yellow	Power is not present System is powered on System power fault detected
Alarm (ALM)	Off Red	Normal operation Alarm State on the Alarm Input
VPN	Off Green	No VPN tunnel At least one VPN tunnel is up
USB CONS	Off Green	RS232 Console Port is active. USB Console port is inactive. USB Console port is active. RS232 Console port is inactive.

LED	Color	Description
SSD	Off Flashing Green	No SSD Activity SSD Activity Detected
RSVD	Yellow Green	Reserved
RSVD	Yellow Green	Reserved

In addition, eight more LEDs are defined, one each for the 6 GE ports, and two for the 2 SFP ports. See the following table.

LED	Color	Description
GE 1/0 LAN	Off Green Flashing Green	No Link Link Activity
GE 1/1 LAN	Off Green Flashing Green	No Link Link Activity
GE 1/2 LAN	Off Green Flashing Green	No Link Link Activity
GE 1/3 LAN	Off Green Flashing Green	No Link Link Activity
GE 0/0 WAN	Off Green Flashing Green	No Link Link Activity
GE 0/1 WAN	Off Green Flashing Green	No Link Link Activity
SPF 0/0 WAN	Off Yellow Flashing Yellow	No Link Link Activity

LED	Color	Description
SPF 0/1 WAN	Off Yellow Flashing Yellow	No Link Link Activity

Note There is no Link Speed indicator signal for LED on ESR board. Instead, software must read the internal ESR Ethernet registers to report the speed of the link. Cisco has standardized the ESR design to report "Link Established" and "Link Traffic Activity" on a single LED, but not Link speed.

Block Diagrams

System integrators can find block diagrams that represents how the ESR board connects into their system located here:

- Basic GigE Router
- Basic GigE Router with SFP WAN
- Console Port Options
- GigE Router with no PoE
- GigE Router with PoE+

Mechanical and Environmental Testing

The tests listed in the following table were successfully executed on the conduction-cooled models of the Cisco ESR6300. These tests used a representative enclosure that conforms to the mounting and thermal mechanisms shown in Thermal Design Considerations, on page 37. Because this type of testing is highly dependent on factors such as the test enclosure design, the thermal solution, the front panel connectors, and the mounting, the following test results should only be used as a reference.

Table 5: Tempurature

High and Low Temperature Cycle Stress (Operational)	High Temperature: 74°C (165°F) Low Temperature: -40°C (-40°F) Reference: MIL-STD-810F, Method 501.4, Procedure II and Method 502.4, Procedure II; SAE J1455 (Rev AUG94), Section 4.1.3

Thermal Shock (Non-Operational)	High Temperature: 85°C (185 °F) Low Temperature: -40°C (-40 °F) Cycle: 2 hours high temperature, 2 hours low temperature Test Period: 2 hour pre-soak at low temperature, followed by 5 cycles Repetition: 5 test periods Reference: MIL-STD-810F, Method 503.4; SAE J1455 (Rev AUG94), Section 4.1.3.2
High Temperature Component Thermal Test (Operational)	Method: Thermocouples on all critical/hot components at board level. Bring temperature of top center surface of thermal plate to 85°C (185 °F) and allow it to stabilize. Ensure that all components are within manufacturer thermal specifications.

Table 6: Altitude

Low Pressure/Altitude (Operational)	Altitude: 4,572m (15,000ft) Equivalent Absolute Pressure: 57.2 kPa (8.3 lbf/in2) Temperature: -40°C (-40°F) to 74°C (165°F) Altitude Ramp Rate: 10m/s (max) Temperature Ramp Rate: 1.5°C (min) to 4.5°C (max) Reference: MIL-STD 810F, Method 500.4, Procedure II; SAE J1455 (Rev AUG94), Section 4.1.3.1
	Altitude: 12,192m (40,000ft) Temperature: 25°C (77°F) ambient
Low Pressure/Altitude (Non-Operational)	Altitude: 12.2km (40,000 ft) Equivalent Absolute Pressure: 18.6kPa (2.7lbf/in2) Temperature: -40°C (-40°F) to 85°C (185°F) Altitude Ramp Rate: 10m/s (max) Temperature Ramp Rate: 1.5°C (min) to 4.5°C (max) Reference: MIL-STD-810F, Method 500.4; SAE J1455 (Rev AUG94), Section 4.1.3.1

Table 7: Humidity

Temperature & Humidity Cycle Stress (Non-Operational; Energized)	Humidity: 95% +/- 5% RH Pressure: 103.4 kPa (15 lbf in2) Temperature: -40°C (-40°F) to 65°C (149°F) Cycle: One, 24 hour cycle Reference: SAE J1455 (Rev AUG94), Section 4.2.3
Active Temperature/Humidity 10 Day Soak (Non-Operational; Energized)	Temperature: -40°C (-40°F) to 65 °C (149 °F) Humidity: 95% +/- 5% RH Cycle: Ramp from 25°C to -40°C over 75 minute period, dwell at -40°C for 240 minutes, ramp to 65°C over 120 minute period, dwell at 65°C for 240 minutes (95% +/- 5% RH), ramp to 25°C over 45 minute period, dwell at 25°C for 120 minutes (50% +/- 5% RH) Repetition: 20 total cycles (10 days total) Reference: MIL-STD-810F, Method 507.4; SAE J1211 (Rev NOV78), Section 4.2.2; SAE J1455 (Rev AUG94), Section 4.2.3

Table 8: Vibration

Random Vibration (Operational)	Acceleration: 1.04g rms vertical, 0.204g rms transverse, 0.740g rms longitudinal Duration: 2 hours per axis Test orientation: 3 axes Reference: MIL-STD-810F, Method 514.5, Category 4

Table 9: Shock

Crash Hazard Shock (Non-Operational)	Acceleration: 75G Duration: 8-13ms Test orientation: 3 axes (positive and negative) Number of shocks: 2 shocks in each direction, 12 shocks total Reference: MIL-STD-810F, Method 516.5, Procedure V

Functional Shock (Operational)	Acceleration: 40G Duration: 15-23ms Test orientation: All 6 faces, in 3 perpendicular axes Reference: MIL-STD-810F, Method 516.5, Procedure I
Bench handling shock (tip) (Operational)	Test orientation: All four edges of each face to form 10° angle with bench top Reference: MIL-STD-810F, Method 516.5, Procedure VI

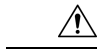
Overtemperature Detection

The ESR Board has a temperature sensor mounted on the edge of the board and thermally attached to the cooling plate. The location is U23, and identified as Thermometer in Thermal Design Considerations.

The digital temperature sensor measures the temperature of the conduction plate (or the integrators equivalent of the conduction plate), not the local ambient temperature. The product datasheet states the board will operate as long as the conduction plate is in the range of -40C to +85C. The alarms are set accordingly and will generate a syslog message, however, there is no SNMP trap.

The high temperature alarm thresholds are set as follows:

- Minor alarm at +80C the conduction plate temperature is close to the rated thermal limit of the unit, and will notify the user. The components are still within the specification, so there is no degradation to the long term reliability of the system.
- Major alarm at +90C the conduction plate temperature is over the rated thermal limit of the unit, and will notify the user. This will impact the long term reliability of the system.
- Critical alarm at +96C the conduction plate temperature is way over the rated thermal limit of the unit, and will notify the user. This will impact the long term reliability of the system. For the Critical Alarm threshold to be reached, it means that the ambient temperature of the system will be exceeded. Hardware failure is immanent, and the failure time will depend upon your installation. Depending on the severity at this point, the failure may be temporary or permanent.



Caution IOS will never shut down a device because the temperature exceeds the specification. Cisco does not guarantee the functionality, nor the long term reliability of a device operating beyond Cisco specifications, but lets the device continue operating until some piece of hardware physically shuts down. Operating outside of the temperature specifications will void the product warranty.

The status of the temperature sensors can be reported from the Cisco ESR6300 command line interface:

```
router# show environment all
ALARM CONTACT 1
   Status:      not asserted
   Description: external alarm contact 1
   Severity:    minor
   Trigger:     closed
ALARM CONTACT 2
```

```
   Status:      not asserted
   Description: external alarm contact 2
   Severity:    minor
   Trigger:     closed
Supervisor Temperature Value: 51 C
Temperature State: GREEN
System Temperature thresholds
------------------------------
Minor Threshold    : 80 C (Yellow)
Major Threshold    : 90 C (Red)
Critical Threshold : 96 C
Shutdown Threshold : 105 C
Pwr Supply         Type     Status
------------------------------------
POWER SUPPLY-A      DC      OK
POWER SUPPLY-B      DC      OK
```

Configuration Reset Overview

The push button input present in the Cisco ESR6300 Series, helps in the quick recovery of the router. Use this feature to recover your router that is hung or stuck. Press the push button and boot the preconfigured “golden.bin” image and “golden.cfg” configuration.

The push button can be actuated only during the hardware initialization stage, after power-on, or at the reload command. The Reset button can not be used once the router gets into the Rommon mode or the IOS mode.

Note Configure a fall-back image with the name “golden.bin” (bootflash:); and a fall-back configuration with the name “golden.cfg” (bootflash: or nvram:). The partner / integrator must have added this optional feature to their carrier board to use the Configuration Reset and / or Zeroize features.

Example Command Line Output

```
ESR6300#write erase
*********************************************************************************************
Erasing Nvram will not clear license trust code.
*********************************************************************************************
Erasing the nvram filesystem will remove all configuration files! Continue? [confirm]
[OK]
Erase of nvram: complete
ESR6300#
Sep 10 21:06:38.209: %SYS-7-NV_BLOCK_INIT: Initialized the geometry of nvram

ESR6300#show start
startup-config is not present. <-Confirmation that the startup configuration is gone.

ESR6300#dir
Directory of bootflash:/
150177  drwx      151552  Sep 10 2021 21:07:07 +00:00  tracelogs
15809   drwx        4096  Sep 10 2021 21:06:38 +00:00  .dbpersist
102753  drwx        4096  Sep 10 2021 21:03:34 +00:00  .installer
126465  drwx        8192  Sep 10 2021 21:02:32 +00:00  license_evlog
158081  drwx        8192  Sep 10 2021 21:02:29 +00:00  its
13      -rw-          30  Sep 10 2021 21:02:14 +00:00  throughput_monitor_params
23      -rw-      5242880  Sep 10 2021 21:01:38 +00:00  ssd
```

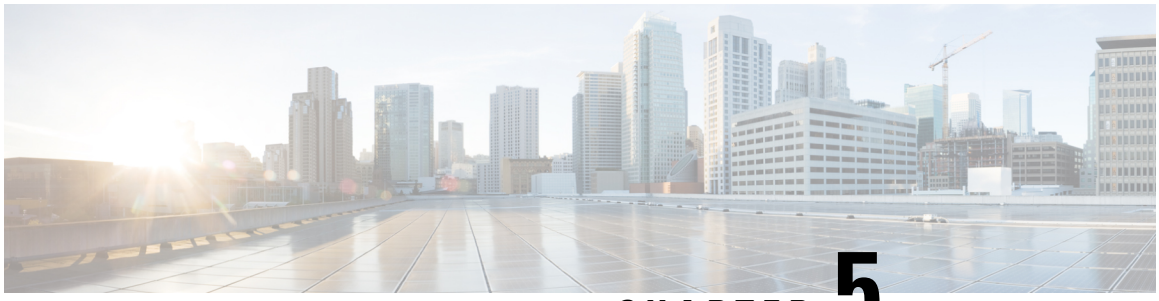
```
12      -rw-         156  Sep 10 2021 21:01:17 +00:00  boothelper.log
19      -rw-        16106  Sep 10 2021 21:01:08 +00:00  mode_event_log
118562  drwx        4096  Sep 10 2021 20:57:45 +00:00  pnp-tech
142274  drwx        4096  Sep 10 2021 20:57:01 +00:00  pnp-info
118561  drwx        4096  Sep 10 2021 20:56:54 +00:00  .prst_sync
11      -rw-         156  Sep 10 2021 20:55:56 +00:00  boothelper.old
28     -rw-      10855  Sep 10 2021 20:52:03 +00:00  golden.cfg <-The original configuration
 was saved here. You MUST use "golden.cfg".
25      -rw-   633006165  Jul 27 2021 19:25:19 +00:00  c6300-universalk9.17.06.01.SPA.bin
47425   drwx        4096  Jul 27 2021 19:09:38 +00:00  core
17      -rw-   633021206  Jul 27 2021 17:03:51 +00:00
c6300-universalk9.BLD_V176_1_THROTTLE_LATEST_20210716_141617_V17_6_0_135.SSA.bin
16      -rw-            14294  Apr 26 2021 23:04:15 +00:00  CCME_Lab_config.txt
 --More--
```

Pushbutton held for 5 seconds after power up while power is applied

```
System Bootstrap, Version 3.4(REL), RELEASE SOFTWARE
Copyright (c) 1994-2021  by cisco Systems, Inc.
ESR-6300-CON-K9 platform with 4194304 Kbytes of main memory
MCU Version - Bootloader: 8, App: 10
MCU is in application mode.
Reset button push detected. <- The bootloader detected the pushbutton pressed.
unable to open bootflash:golden.bin (14)
```

After the system has finished rebooting, the startup and running configuration will have what was stored in "golden.cfg".

```
License Usage
=============
network-essentials_250M
(ESR6300_P_250M_E):
  Description: network-essentials_250M
  Count: 1
  Version: 1.0
  Status: IN USE
  Export status: NOT RESTRICTED
  Feature Name: network-essentials_250M
  Feature Description: network-essentials_250M
  Enforcement type: NOT ENFORCED
  License type: Perpetual
```



CHAPTER 5

Device Zeroization

This chapter contains the following sections:

Device Zeroization

Zeroization consists of erasing any and all potentially sensitive information in the router. This includes erasure of Main memory, cache memories, and other memories containing packet data, NVRAM, and Flash memory. The process of zeroization is launched upon the initiation of a user command and a subsequent trigger.

By default, the router will have the zeroization feature disabled. SPI: Flash, I2C, and ACT2 are not impacted by this feature.

When zeroization is functionally active, the SYS LED indicates blinking yellow until the router reloads.

Important In order to recover the device from a complete zeroization, it must be configured with a Cisco supported USB3.0 device.

Caution The ESR6300 does not support USB hot plug when it is in ROMMON mode.

Push Button

There is no actual button on the ESR6300, and the system integrator must configure their platform with a Push Button. Reset on an ESR6300 does not cause the device to reboot, but initiates the configured level of zeroization.

Zeroization can be triggered by the Push Button, or software-triggered by a privilege 15 user with console access. There is no remote access for security reasons.

On the router, the Push Button is used exclusively for triggering the Zeroization process which will zeroize and erase switch configuration files or entire flash file system depending on the option provided under the CLI command **service declassify**.

The Zeroization process starts as soon as the Push Button is pressed. The CLI command, **service declassify**, is used to set the desired action in response to the Push Button press. To prevent accidental erasure of the system configuration/image, the default setting is set to **no service declassify**.

Important Notice about Zeroization

eMMC is a managed NAND. This means that the router system does not interact with the flash memory directly. The flash controller presents a block-style interface to the system, and it handles the flash management (analogous to the Flash Translation Layer). The embedded router system cannot access the raw flash directly.

The JEDEC standard has commands that are supposed to remove data from the raw flash. In Cisco's implementation, the "Erase" and "Sanitize" commands are used. The eMMC standard JESD84-B51 defines "Sanitize" as follows:

"The Sanitize operation is a feature ... that is used to remove data from the device according to Secure Removal Type. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space".

After the sanitize operation is completed, no data *should exist* in the unmapped host address space.

Warning Zeroization does NOT erase removable media such as SD Card and USB Storage. This media must be removed from the system and erased or destroyed using procedures that are outside the scope of this document.

Warning Zeroize does a very thorough wipe of all non-protected parts of the eMMC flash using the best technology designed by the flash manufacturer today and can do so using the push of a button without the need for a console, ssh, or management session of any kind. It is the integrator's and end user's responsibility to determine the suitability regardless of the CLI keyword used to enable the feature.

Warning While Cisco IOS and Cisco IOS-XE use the command line text of "declassify" in the command line interface (CLI) to enable the zeroize feature, in no way does this represent any specific endorsement or acknowledgment of a Government approved flash erasure methodology.

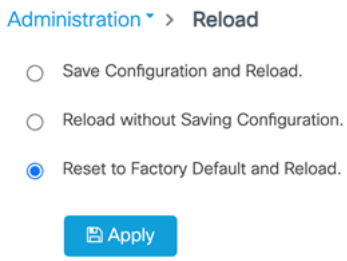
Warning Declassification procedures are unique to each Government organization. Cisco solely provides the technical detail of the erasure operation here, not the policy distinction or any specific recommendation per classification.

Warning Please refer to your respective Government Agency policies, procedures, and recommendations for the handling of sensitive data to see if this procedure meets with those requirements.

WARNING!

The CLI **service declassify erase-all** is literally a **software self-destruct mechanism** intended for defense and intelligence environments that attempts to wipe clean, all of the writable non-volatile storage on the device to clear the device configuration, other stored configurations and all security credentials including any additional license keys.

Please do not use this feature in lieu of doing a **write erase** from the CLI or from the Administration page, Reload option of the WebUI. Invoke the reload with the **Reset to Factory Default and Reload** option and click **Apply**. See the following figure.



If **service declassify erase-all** is invoked, after restoring the IOS-XE image and device configuration, you must re-license the device using the standard Cisco Smart Licensing procedures which ultimately require a Cisco Smart Account and access to the internet or a satellite license server.

Zeroization Details

These are the detailed steps the ESR6300 software performs after pressing the Push Button with **service declassify erase-all** enabled:

Zeroization is triggered after push button is pressed for 4 seconds:

1. Software will check if **service declassify erase-all** is enabled in the configuration. If not enabled, then nothing happens. If it is enabled, then will move on to the next step.
2. Software deletes vlan.dat, nvram_config, moncfg, and NVRAM partition. Then software sanitizes the eMMC which is the storage device permanently soldered to the ESR6300 module.
3. Software removes all rommon variables, but it will set one rommon variable to tell bootloader to finish the rest of zeroization process. Eventually that rommon variable will be removed by bootloader after it finishes zeroization.
4. A software trigger is set to soft reload the system. Control is passed to the bootloader.

Zeroization Performed on bootloader:

1. After display banner is in rommon, it will then read the rommon variable flag. If the flag exists, then it will finish the rest of zeroization by executing the erase and sanitize commands to the eMMC device. This results in the bootflash partition being removed.
2. Next, it removes the rommon variable flag if zeroization was successful and it will go back to the rommon CLI prompt.

Note If a power cycle happens during zeroization, the bootloader would start zeroization over again since the rommon variable for zeroize is still present.

The following message appears on the console when reset has been triggered:

```
System Bootstrap, Version 1.4(DEV) [vandvisw-vandvisw 113], DEVELOPMENT SOFTWARE
Copyright (c) 1994-2019 by cisco Systems, Inc.
Compiled at Mon Jun 3 10:56:19 2019 by vandvisw
ESR-6300-CON-K9 platform with 4194304 Kbytes of main memory
MCU Version - Bootloader: 8, App: 10
MCU is in application mode.
Reset button push detected
```

Zeroization Trigger

Zeroization can be triggered by either software or by the Push Button. In either case, there are a series of commands that need to be entered.

```
Router#config terminal
Router(config)#service declassify {erase-nvram | erase-all}
```

To confirm if the option is enabled:

```
Router#show declassify
Declassify facility: Enabled=Yes  In Progress=No
  Erase flash=Yes  Erase nvram=Yes
  Declassify Console and Aux Ports
  Shutdown Interfaces
  Reload system
```

To remove the option, use the following command:

```
Router(config)#no service declassify
```

To Trigger Zeroization

To trigger the zeroization from the command line:

```
Router#declassify trigger
```

To trigger the zeroization from the Push Button, press and hold the button for 4+ seconds. When the system auto reloads, it will come up in ROMMON mode: "$$" with bootflash: wiped clean.

Command Line Interface

There are two levels of zeroization actions, erase-nvram and erase-all. The following CLI shows the options:

```
router(config)#service declassify ?
erase-nvram    Enable erasure of router configuration as declassification action. Default
is no erasure.
erase-all      Enable erasure of both flash and nvram file systems as part of
declassification. Default is no erasure
```

Microcontroller Unit (MCU)

The MCU is part of the ESR6300 hardware. It performs the following functions:

- Monitors the Push Button status at power up
- Monitors the system hardware watchdog output
- Maintains Reset Reason register
- Controls the SYS LED

The MCU versions are displayed using show version. Details on MCU version and upgrade status are also stored in Flash: as boothelper.log. The MCU is automatically upgraded by the software.

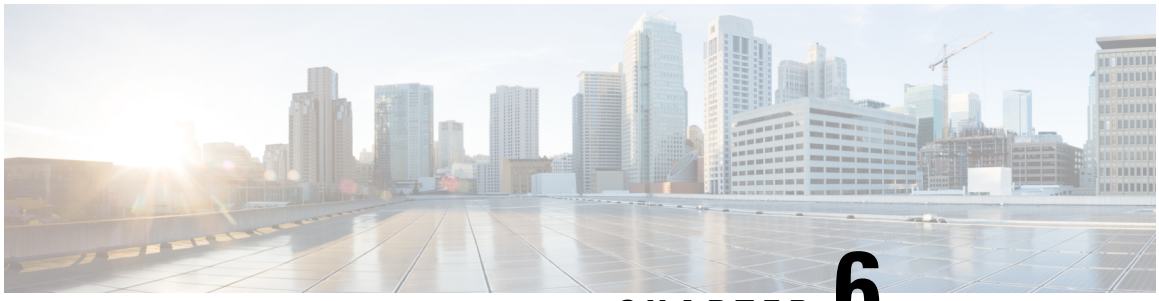
```
Router#show ver | i MCU
MCU bootloader version: 8
MCU application version: 10

Router#cat flash:boothelper.log
Logging at Fri Nov 15 05:00:54 Universal 2019
boot loader upgrade enabled
Bootloader is up-to-date
Current MCU App version is 10
MCU firmware is up-to-date
```

In the event the MCU Application is corrupt, or does not match the Release Notes version, this has to be repaired. Steps to recover from this state: Reload router, hit Ctrl+C to break into rommon mode.

```
Rommon>set MCU_UPGRADE=IGNORE<- Ignore MCU firmware upgrade errors.

Rommon>sync

Rommon>reset

Rommon>boot bootflash:<image>
```

Once the MCU successfully upgrades, you can disable/unset this IGNORE option in rommon. Details on other MCU setting rommon options follow: (there are no available IOS configuration options or linux shell mode troubleshooting measures)

```
set MCU_UPGRADE=SKIP <- Prevents MCU firmware upgrade from taking place.

set MCU_UPGRADE=FORCE <- Forces MCU firmware upgrade to take place.

unset MCU_UPGRADE <- Normal operation. Allows automatic upgrade.
```



CHAPTER 6

Appendix

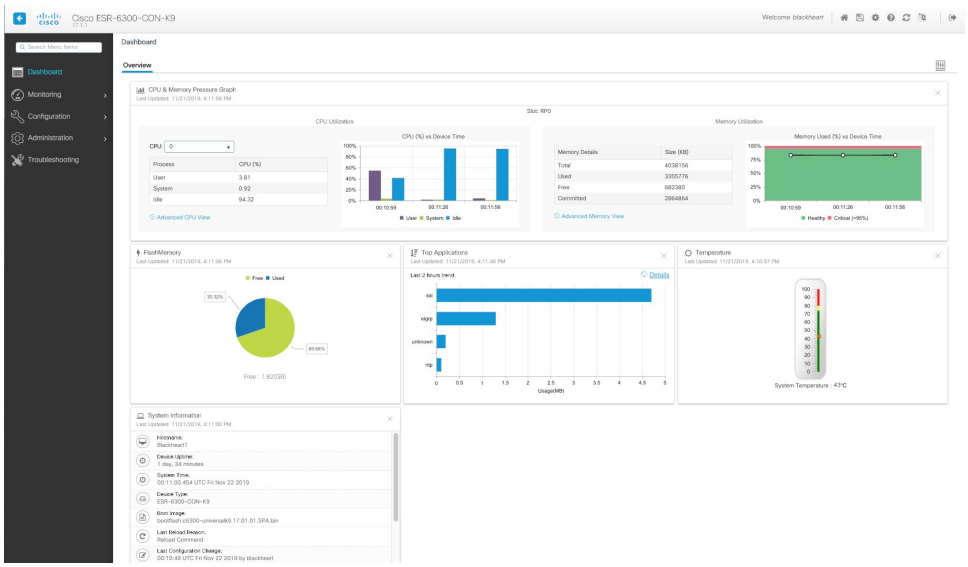
This chapter contains the following sections:

Web User Interface

The Cisco IOS-XE operating system provides a graphical user interface for monitoring and configuration of your device. The WebUI needs to be enabled before it can be used. Use these commands to enable it:

```
username admin privilege 15 password 0 passwordname
ip http server
ip http authentication local
ip http secure-server
```

When launched, the initial display is a dashboard that looks similar to the following example:



Compliance and Safety Information

The ESR6300 was installed in a representative chassis, tested, and shown to meet the standards listed in the following table. Individual results will depend on final implementation. Formal compliance testing must be performed by the integrator in a fully assembled product.

Specification	Description
Safety	• UL 60950-1 Recognized Component (R/C) • CSA22.2-No. 60950-1 • EN60950-1 • IEC60950-1
Emissions	• EN 55022 / CISPR 22 • EN 55032 / CISPR 32 • FCC Part 15 Subpart B • ICES 003 for class A device
Immunity	• EN 55024 • EN 55035 • EN 61000-4-2 • EN 61000-4-3 • EN 61000-4-4 • EN 61000-4-5 • EN 61000-4-8 • EN 61000-4-16 • EN 61000-4-18

RoHS (Restriction of Hazardous Substances)

RoHS is directive being adopted worldwide that restricts certain limits of the following materials from certain manufactured products:

- Lead (Pb): < 1000 ppm
- Mercury (Hg): < 100 ppm
- Cadmium (Cd): < 100 ppm
- Hexavalent Chromium: (Cr VI) < 1000 ppm
- Polybrominated Biphenyls (PBB): < 1000 ppm
- Polybrominated Diphenyl Ethers (PBDE): < 1000 ppm

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Related Documentation

Cisco ESR6300 Embedded Series Router

ESR6300 documentation landing page

Product Independent Documentation

Cisco Industrial Routers and Industrial Wireless Access Points Antenna Guide

Cisco IOS XE 17.x

Cisco SD-WAN

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